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17 February 1984

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WEATHER ROCKET LAUNCHING PAD--The first Bulgarian launching pad for meteorological rockets was put into operation near the Black Sea city of Akhtopol. Rocket number one was fired to an altitude of 100 kilometers. Atmospheric layers of up to 200 kilometers, located below the range of weather satellites, can be explored using additional probes. The measurements gained from meteorological rockets will considerably improve long-term prognoses for industry and agriculture. [Text] [East Berlin TRIBUENE in German 16 Jan 84 p 4]

CSO: 2302/20

DESCRIPTION OF 8048 MICROCOMPUTER OPERATION PUBLISHED

Prague SDELOVACI TECHNIKA in Czech No 8, 1983 pp 283-300

[Article by Eng Michal Cernoch, Eng Zdenek Stehno, and Eng Vlasta Vybulkova: "The 8048 Microcomputer"]

[Text] Introduction

The rapid development of production technology for unipolar integrated circuits is allowing their qualitative and quantitative characteristics to be steadily improved. Practical consequences include the implementation of increasingly complex and powerful circuits, and a considerable drop in the prices of relatively simple circuits as a result of the profitability of mass production. This creates favorable conditions for further expansion of the utility of microelectronic components in new and quite nontraditional production sectors. General-purpose integrated circuits whose functions can be changed by changing the control program are the most adaptable to varied application requirements. Monolithic microcomputers are typical representatives of such circuits. Every important producer offers microprocessors for use in applications where a microprocessor-based microcomputer system would be too complex and expensive and accordingly not usable.

The Series 48 Integrated Microcomputers

A large series of integrated microcomputers, of which the 8048 is a typical representative, supplemented the 8080A and 8085 8-bit microcomputer program. The characteristics of the other members of the series differ only in a few respects which are not important in terms of internal structure. Obviously this statement should not be taken entirely literally: certain types of microcomputers may operate with the same or a largely similar instruction set but not be equipped with the same hardware. Accordingly, their specific properties will differ in some respects. The main characteristics of the 48 series are presented in Table 1.

Microcomputers with characteristics equivalent to those of the 8048, 8748 and 8035 are being prepared for production in Czechoslovakia. Implementation of the 8748 microcomputer with EPROM [erasable programmable read-only memory] will come later than the actual availability of the 8048 and 8035 as a result of the great technical difficulty involved. In addition, we

must bear in mind that the only difference between the 8048 and 8035 microcomputers is that the 8048 has an active ROM [read-only memory] internal memory with a capacity of 1024 x 8 bits, which is programmed by a single process mask during production. The 8035 is in fact only a special functional state of the 8048.

Table 1. Basic Characteristics of 48 Series Integrated Microcomputers

a Typ	b Int. paměť ROM/EPROM	c (byty) RWM	d Doba cyklu [us]	e Počet kanálů V/V (bit)	f Vnější přerušení	g Interní čítač	h Možnost rozšíření	i Převodník A/Č	j Pouzdro DIL
8048	1024 ROM	64	2,5	3 × 8	ANO	ANO	ANO	NE	40
8035	—	64	2,5	3 × 8	ANO	ANO	ANO	NE	40
8748	1024 EPROM	64	2,5	3 × 8	ANO	ANO	ANO	NE	40
8049	2048 ROM	128	1,4	3 × 8	ANO	ANO	ANO	NE	40
8041	1024 ROM	64	2,5	4 × 8	NE	ANO	NE	NE	40
8741	1024 EPROM	64	2,5	3 × 8	NE	ANO	NE	NE	40
8021	1024 ROM	64	10	2 × 8 + 1 × 4	NE	ANO	NE	NE	28
8022	2048 ROM	64	10	3 × 8	NE	ANO	NE	ANO	40

Key:

a. Type
b. ROM/EPROM internal memory
c. Bytes of RWM [read-write memory]
d. Cycle time (ns)
e. Number of I/O channels (bits)
f. External interrupt
g. Internal counter-timer
h. Expandable
i. Analog-digital converter
j. DIL package [no. of pins]

ANO = Yes
NE = No

Main Characteristics of the 8048 Microcomputer

The 8048 integrated microcomputer will be produced in Czechoslovakia with unipolar technology using n-type transistors with polycrystalline silicon gates. The load transistors of the individual logic gates work in the depletion mode. More than 20,000 transistors are integrated onto a chip surface measuring 5.2 x 5.4 mm. This is a nearly fourfold increase in density over the 8080A (200 components per mm^2 in the 8080A, 760 components per mm^2 in the 8048).

The 8048 microcomputer is packaged in a 40-pin DIL [dual in-line] package with the pin assignments as shown in Fig. 1. The functions of the individual pins are briefly described in Table 2.

The specific logical, arithmetic and other circuit functions in the 8048 microcomputer are realized in a manner very similar to that used in the 8080A and described in detail in Ref. 5. Accordingly we will keep detailed description of the functions of typical elements of the microcomputer to a minimum. We will go into more detail only regarding the parts of the microcomputer which are of interest to the user (design of I/O [input-output] channels, interrupt handling, special functional states, and control of the internal oscillator).

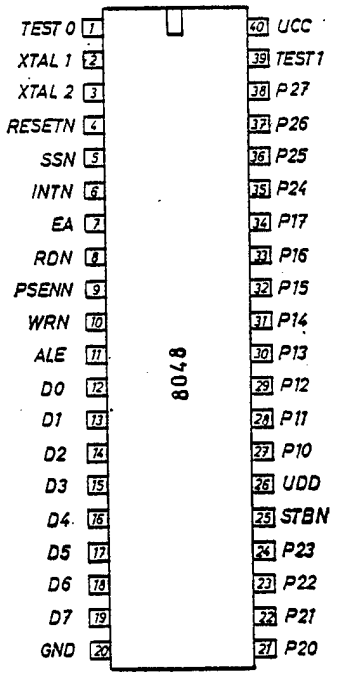


Fig. 1. Pin Assignments of 8048 Microcomputer

Table 2. Brief Description of Functions of Pins of 8048 Microcomputer

Signál	a	b Funkce
RESETN	c	nastavuje výchozí stav obvodu; specifické použití v režimu čtení obsahu vnitřní paměti programu (ROM)
XTAL1,2	d	připojení krystalu, členu LC nebo vstup vnějších hodin
ALE	e	periodický signál, který se především používá pro zápis adresy externí paměti programu nebo dat do vyrovnávacího registru (*A*dress *L*atch *E*nable)
PSENN	f	signál, který povoluje přenos z externí paměti programu (*P*rogram *S*torage *EN*able)
WRN	g	signál, kterým je výstup kanálu *0* (*D7* až *D0*) zapsán do vnější paměti dat nebo registru vazebního obvodu
RDN	h	signál, kterým je na vstup kanálu *0* připojena externí paměť dat nebo data z vazebního obvodu
INTN	i	externí žádost o přerušení běhu programu
TEST0	j	vstup, jehož stav lze testovat programem; ve zvláštním režimu je vývod zapojen jako výstup interního hodinového signálu *FV*
TEST1	k	vstup, jehož stav lze testovat programem nebo je určen jako vstup čítače událostí
SSN	l	vstup, jenž umožňuje krokovat zpracování programu po instrukcích
EA	m	vstup, jenž umožňuje odpojit interní paměť programu (8048 — 8035) — použití při ladění i diagnostice
D7 ÷ D0	n	kanál *0* s třístavovými výstupy; činnost je synchronizována se signály *RDN*, *WRN*, *ALE* a *PSENN*. Stav výstupů může být pamatován ve výstupní vyrovnávací paměti
P17 ÷ P10	o	kanál *1* s výstupní vyrovnávací pamětí a s možností nastavit jednotlivé bity do funkce vstupu nebo výstupu
P23 ÷ P20	p	dolní polovina kanálu *2* zabezpečuje spolupráci s expandérem typu 8243 a adresování externí paměti programu, funkční vlastnosti shodné s kanálem *1*
STBN	q	signál, který řídí přenos dat mezi mikropočítačem a expandérem 8243
P27 ÷ P24	r	horní polovina kanálu *2* má shodné funkční vlastnosti jako kanál *1*

[Table 2 continued on following page]

UCC	s	napájecí napětí +5 V
UDD	t	napájecí napětí +5 V v případě výpadku zdroje napětí *UCC*
GND	u	potenciál země 0 V

Key:

a. Signal
b. Function
c. Initializes circuits; specific uses in internal program memory (ROM) read mode
d. Connection of crystal, LC circuit or external clock input
e. Periodic signal used primarily for moving address of external program memory or data memory to buffer (Address Latch Enable)
f. Signal enabling transmission from external memory (program storage enable)
g. Signal which causes output of channel 0 (D7-DO) to be written into external data memory of interface register
h. Signal which connects external data memory or data from interface to input of channel 0
i. External interrupt request
j. Input whose state can be tested by software; in a special mode, the pin is connected as output of internal clock signal FV
k. Input whose state can be adjusted by software or is specified as input of event counter
l. Input allowing single-stepping of program
m. Input allowing disconnection of internal program memory (8048-8035), used in debugging and diagnostics
n. Channel 0 with 3-state output; activity synchronized with signals RDN, WRN, ALE and PSENN; state of outputs may be stored in output buffer
o. Channel 1, with output buffer and capability of setting individual bytes for input or output function
p. Lower half of channel 2, allowing operation with 8243 expander and addressing of external program memory; functional capabilities same as channel 1
q. Signal which controls data transmission between microcomputer and 8243 expander
r. Upper half of channel 2; same functional capabilities as channel 1
s. +5 V power supply
t. +5 V power supply used during outage of UCC
u. Ground potential, 0 V

The 8048 may work completely independently, or its functional capabilities may be expanded by adding external circuits with a wide range of functions. It is easy to connect it to most of the auxiliary circuits intended for systems using the 8080A and 8085 microprocessors. The specific expansion requirements and possibilities will be discussed during analysis of the 8048's internal structure and the processing of certain instructions or special functional states.

Block Structure of the 8048

The internal structure of the 8048 integrated microcomputer is shown in Fig. 2. The transmission paths between the individual blocks are represented by the customary arrowheads, in addition to which the names of the internal signals which cause the relevant data transfers are given. The control signals are generated by the control unit; their names are generally mnemonic abbreviations of the operation names (WSWDB = "Write Status Word on Data Bus").

The great majority of data transfers between blocks of the microcomputer are carried out via the internal bus, DB7-DB0. Table 3 shows the permissible waveforms of the most important control signals and briefly describes their functions in the 8048 microcomputer. There may be minor differences in some of the signals under special circumstances; when necessary these will be specially noted. If a given signal is active when it is at the L [low] logical level, its abbreviation ends in the letter N ($\overline{RD}$ = RDN, $\overline{PSEN}$ = PSENN and so on). We should also note that this microcomputer is not a von Neumann machine, because the program memory is separated from the data memory.

The operation of the microcomputer results from execution of a program stored in program memory. The program consists of a set of instructions and program constants (immediate data). The instruction determines unambiguously the behavior of the microcomputer during its execution (instruction cycle). An instruction may be 1 or 2 bytes long and its execution may require 1 or 2 machine cycles (M1, M2). Each machine cycle consists of clock periods T1-T5, and each clock period contains phases FS and FV. During phase FS the internal bus DB is always in the H [high] state and other auxiliary functions are performed (refreshing of data in dynamic memory circuits and the like). The execution phase FV determines the duration of the critical execution signals. The basic signal for the clock circuits is obtained from an internal oscillator. The base frequency may be set precisely by using a given type of crystal (6 MHz), or, in less demanding applications, by means of an LC circuit (3 MHz). The output of a divide-by-3 circuit determines the length of phases FS and FV. The instruction ENTO CLK can be used to feed phase FV to the TESTO output for special purposes. Both phases directly control the operation of the cycle counter, which generates clock periods T1-T5. The functioning of these circuits depends only on provision of the supply voltage V_{CC}. The operation of all other blocks in the microcomputer is controlled by the control unit in accordance with the instruction to be performed or the states of external inputs to it.

It is considerably more difficult to describe the functioning of the 8048 microcomputer than it was in the case of the 8080A. Many of the operations are performed in parallel, and are carried out regardless of whether or not they are important for a particular instruction. They are almost all uninteresting from the user's point of view. Since in general we wish to understand how most of the commonly known principles are specifically implemented in this computer (and in some cases to derive inspiration from their implementation), we must try to understand the functional capabilities of the block diagram of Fig. 2. Below we will give a relatively brief description of the functional capabilities of the individual blocks, with some unavoidable simplifications.

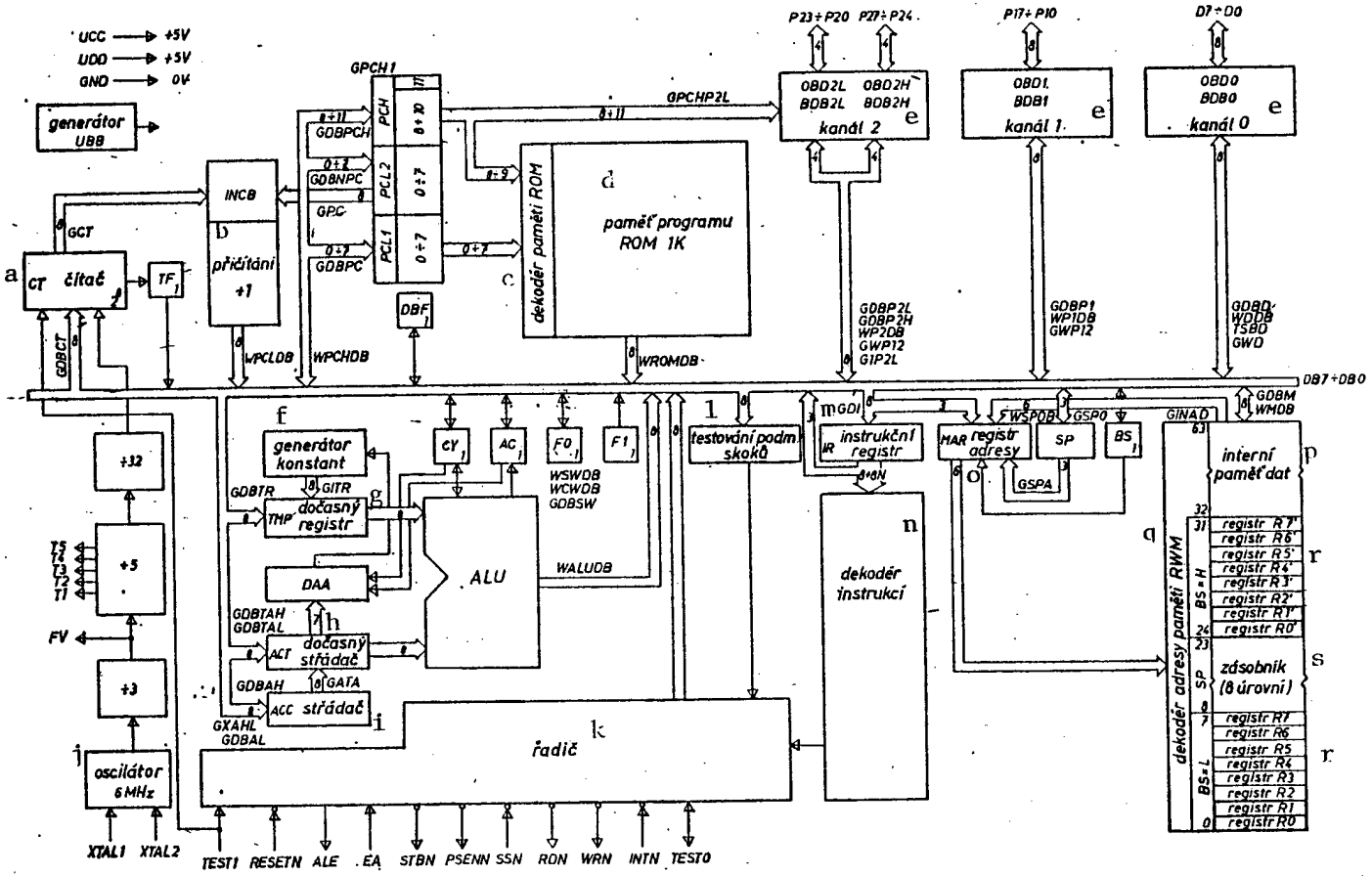
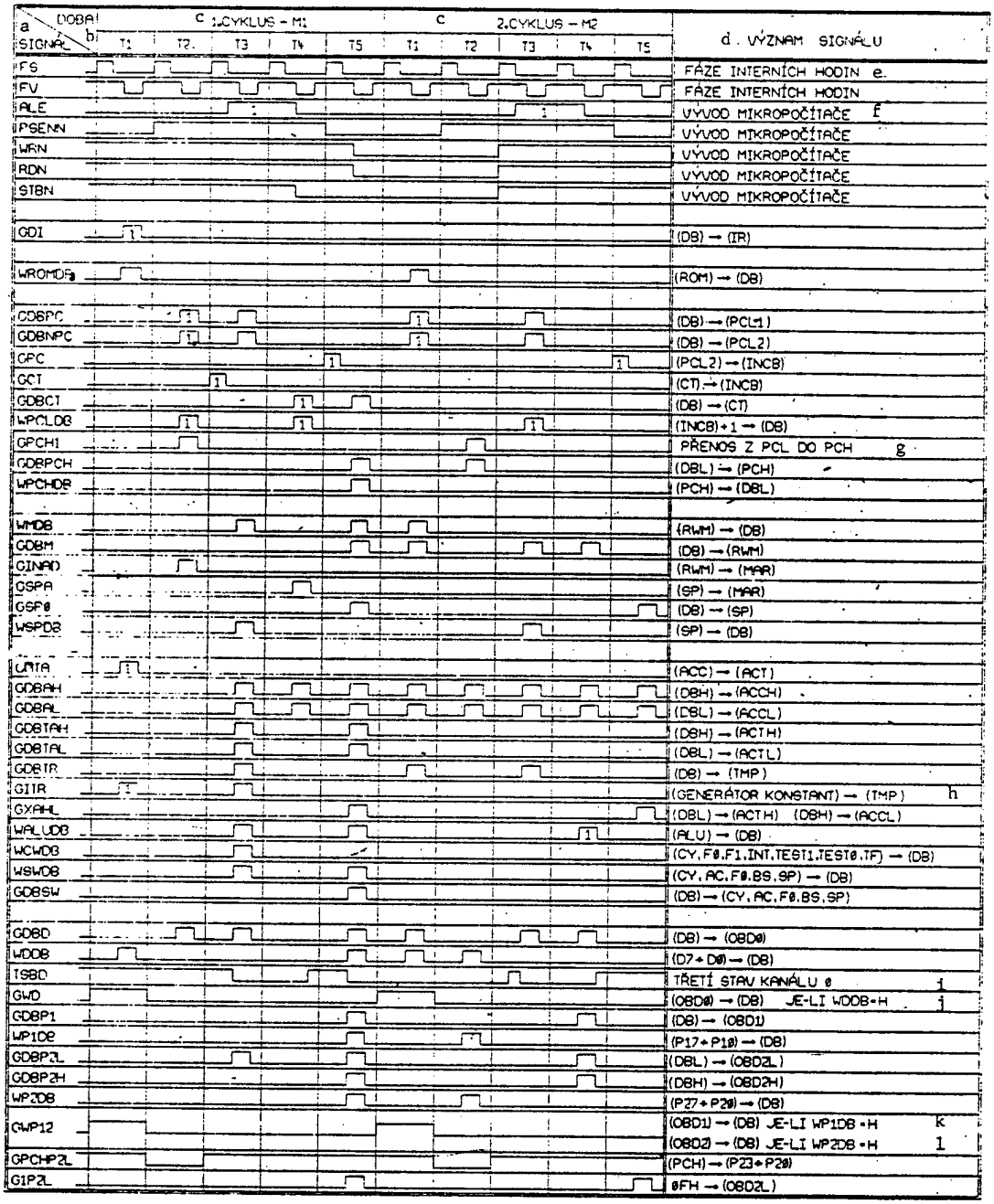


Fig. 2. Structure of 8048 Microcomputer

Key:

a. Counter
b. Increment
c. ROM memory decoder
d. Program memory
e. Channel
f. Constant generator
g. Temporary register
h. Temporary accumulator
i. Accumulator
j. 6 MHz oscillator
k. Control unit
l. Jump condition test
m. Instruction register
n. Instruction decoder
o. Memory address register
p. Internal data memory
q. RWM memory address decoder
r. Registers
s. Stack (8 levels)

Table 3. Functions of Control Signals of 8048 Microcomputer and Possible Waveforms



Key:

a. Signal
b. Clock period
c. Machine cycle
d. Meaning of signal
e. Internal clock phase
f. Microcomputer pin
g. Transfer from PCL to PCH
h. (constant generator) → (TMP)
i. Third state of channel 0
j. if WDDB = H
k. if FWP1DB = H
l. if WP2DB = H

The Arithmetic-Logical Unit (ALU)

The ALU consists only of combinatorial logic circuits, which the control circuit may activate for one of the following functions:

+	arithmetic addition
∧	logical product (AND)
∨	logical sum (OR)
⊕	sum modulo 2 (exclusive OR)
RT	right rotation

The output of the ALU is uniquely determined by the functional connections and the values of the input operands (which are contained in registers ACT and TMP). An additional direct input may come from the carry flag CY. In contrast to the 8080A, it is not possible to create the one's complement of an operand contained in the temporary register, and there is no PCY carry flag. Accordingly, subtraction must be done by software. Since the ALU uses asynchronous saving of outputs as a result of the existence of partial carries, a save period is placed between the clock periods designated for determination of the content of the input operands and reading of the result at the output of the ALU. When the operands are specified in period T1, period T2 is designated for the save operation and period T3 for reading the result. If the results can be read only by activating the WALUDB signal (Write ALU Result on Internal Bus DB), it is possible to backtrack to determine when the input operands would be saved.

The ACC, ACT and TMP Registers

The structure and uses of the registers are very similar to those in the 8080A microprocessor. At the beginning of each instruction cycle, the content of accumulator ACC is written in temporary accumulator ACT and temporary register TMP is cleared. Because there is no direct access to accumulator ACC via internal bus DB, the contents of ACC can be transferred to TMP only via the ALU and its internal bus (adding the contents of the accumulator to zero). One important feature of registers ACC and ACT is that it is possible to operate with either the upper or lower half of their contents. In the mnemonics this is expressed by adding the letter H or L (i.e., GDBAH: write data from DB7-DB4 of internal bus into accumulator bits ACC7-ACC4).

The Constant Generator

The ALU is used for more than just processing arithmetic and logical instructions. This necessitates an extremely flexible ability to change the contents of the temporary register TMP. Accordingly, it can be set without transmission on the internal bus. This considerably speeds up the operation of the microcomputer, since it becomes unnecessary to go through the lengthy process of generating specified constants in software or to include them as program constants [immediate data]. Therefore, the constant generator consists of an ROM auxiliary store which contains the necessary constants. The addresses of the constants are specified by the

control unit and the time at which they are transferred to TMP is controlled by the signal GR. The method of programming the constant generator is shown in Table 4; its practical use will be described later.

Table 4. List of Constants Stored in Generator

	a Váha bitu								b Příklad použití při instrukci
	7	6	5	4	3	2	1	0	
1	0	0	0	0	0	0	0	0	*CLRA, MOV Rr, A*
2	0	0	0	0	0	0	0	1	*INCA, JTF addr*
3	0	0	0	0	0	0	1	0	*JNTO addr*
4	0	0	0	0	0	1	0	0	*JBb addr*
5	0	0	0	0	1	0	0	0	*JT1 addr*
6	0	0	0	1	0	0	0	0	*JNI addr*
7	0	0	1	0	0	0	0	0	*JBb addr*
8	0	1	0	0	0	0	0	0	*JBb addr*
9	1	0	0	0	0	0	0	0	*JC addr*
10	1	1	1	1	1	1	1	1	*CPLA, DECA*
11	0	0	0	0	0	1	1	0	*DAAL*
12	0	1	1	0	0	0	0	0	*DAAH*
13	0	1	1	0	0	1	1	0	*DAA*

Key:
a. Bit weight
b. Example of use in instruction

Instruction Register IR and Instruction Decoder

The opcode of the instruction is contained in the instruction register IR throughout the instruction cycle. The direct and inverted outputs of IR are fed to the instruction decoder, where they activate microinstructions which enable the required control signals to be generated by the control unit. In some special cases the outputs of the IR are used directly by the control unit or form part of data transmitted on the internal bus DB. Specific examples will be described in connection with the instructions CALL or JMP and in analyzing the function of the 8243 I/O expander. If we recall the way in which the instruction register is wired in the 8080A microprocessor, we will note certain differences in the processing of the part of the opcode involving addressing of the instructions in the scratch-pad registers of the internal data memory.

The Program Counter PC and the ROM Program Memory

The 8048 microprocessor contains a 12-bit program counter which can address an ROM [read-only memory] store with a capacity of 4096 x 8 bits. The memory space is divided into pages, which are addressed by the program counter bits designated PCH (maximum 16 pages). Within a page the address is designated by counter bits PCL, i.e., 256 bytes are addressable. The most important of

the PCH bits is PC11, which can be changed only by software. The instructions SEL MB0 or SEL MB1 set flag DBF. The output state of DBF is copied into bit PC11 during the processing of certain instructions. This divides the entire program memory into two halves (memory banks), each with a capacity of 2 Kbyte. In this connection it should be borne in mind that transfers in the program memory address space of the 8048 are subject to certain rules. We will discuss limitations and recommendations in more detail later.

We now turn to the main requirement for the operation of any computer, namely incrementing the program counter PC by 1. The circuits which do this are not very visible and it is difficult to follow their functioning. The reason is that the mechanism for incrementing by 1 is different in the lower half of the counter (PCL) than in the upper part (PCH) (only bits PC10-PC8). PCL is augmented by a block which is also used for augmenting counter CT. This block must be regularly "loaned," which requires that it be provided with its own data buffer INCB (INCrement Buffer). This is very helpful with certain instructions and may make it unnecessary to increment by 1 for the purpose of temporarily saving the contents of PCL.

Actually, counter PCL consists of two 8-bit memories designated PCL1 and PCL2. PCL1 stores the current address of the memory location on the page in question (PC7-PC0), while PCL2 holds the contents of the counter involved in the actual incrementing mechanism. PCL1 has the same contents as PCL2 in almost all instructions. Only the instructions MOVP, MOVP3 and JMPP utilize this apparently redundant circuitry. In processing these instructions we change the content of PCL1 and read in the contents of the addressed program memory location; after execution of the instructions is completed, the program continues with the next following instruction because the content of PCL2 was not changed. We will analyze this situation in more detail when describing the processing of these instructions.

Incrementing program counter PC by 1 begins with reading the contents of PCL2 into buffer INCB by means of signal GPC. If the content of PCL2 is OFFH, a transfer to PCH will be generated by signal GPCH1. The contents of counter PCL are set by transfer of data via bus DB, together with activation of control signals WPCLDB, GDBPC and GDBNPC.

Here we have briefly sketched out the mechanism of classical incrementation of the program counter. This approach modifies certain instructions in various ways, particularly ones that involve another source for the new content of PCL or of the entire counter PC.

It is apparent from the block diagram of Fig. 2 that the 8048 microcomputer contains a 1-Kbyte program memory (1024 x 8 bits). Its address space is covered by program counter outputs PC9-PC0. If the user program is satisfied by this capacity, the situation is relatively simple. There are no difficulties in choosing the memory banks or with the location of the interrupt servicing program. The contents of the addressed program memory location are written on internal bus DB whenever the signal WROMDB is active.

The situation changes considerably if the capacity of the internal program memory is insufficient. Since the address space is available, the capacity may be increased by adding external ROM memory. This requires that we create external data, address and control buses. Another requirement is that we transfer the contents of counter PC to the outputs of the microcomputer so that it can control the address bus. The microcomputer takes care of these requirements automatically as soon as bit PC11 or PC12 is in state H. The content of counter PCL is transferred via internal bus DB to the output buffer of channel 0 (OBD0), while the content of PCH is fed by signal GPCHP2L to outputs P23-P20.

If channel 0 is also designated for transmission of data (in the present case, the instruction opcode or program constants), we must write the address of PCL in another buffer, whose output, together with the output of channel 2L (P23-P20), controls a dedicated address bus. For the period when the address in PCL is being transferred from output buffer OBD0 into auxiliary external storage, the microcomputer generates signal ALE (Address Latch Enable). This specifies the current address of the required memory location in ROM external program memory. The contents of the addressed location are transferred to the external data bus by a signal PSENN (Program Storage ENable Not). This is fed to the CSN (Chip Select Not) pin of the ROM external memory and thus determines the possibility of connection of the memory circuit to data bus D7-D0. The signal PSENN is generated only if access to the external program memory is required. Since the signal EA = H (External Access) disconnects the internal part of program memory, the signal PSENN is generated regardless of the state of bits PC10 or PC11. While the signal PSENN is generated, the data bus transfers the contents of the address location in ROM memory to the input of channel 0 (BDB0). The status at D7-D10 is fed at the proper time to internal bus DB by means of signal WDDB, which preserves the functional equivalence to reading from internal program memory.

Three of the addresses in program memory have a predefined content:

--address 000H contains the beginning of the program for servicing the state of the microcomputer after the end of the signal RESETN = L;

--address 003H contains a jump to the subroutine for servicing an external interrupt request;

--address 007H contains a jump to the subroutine for servicing an interrupt request resulting from a counter/timer overflow.

To utilize the capabilities of the 8048's instruction set, it is advisable to use the zeroth page of internal program memory for various subroutines; the next two pages may be used for the user program, and the third for tables of constants. Fig. 3 shows the addressing capabilities of the program counter PC in the 8048 microcomputer.

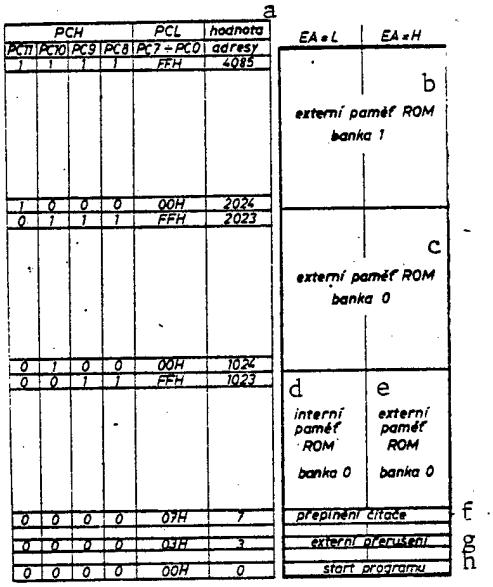


Fig. 3. Addressing Capabilities of Program Counter of 8048 Microcomputer and Structure of ROM Program Memory

Key:

a. Address
b. ROM external memory bank 1
c. ROM external memory bank 2
d. ROM internal memory, bank 0
e. ROM external memory, bank 0
f. Counter overflow
g. External interrupt
h. Program start

We have not yet mentioned the principle by which information is stored in ROM storage. Reading of the contents of the addressed location consists of several phases, during which the sense lines are pulled high, the address decoder is set, the states of the sense lines are set in accordance with the contents of the addressed locations, and the final states of these lines are read onto internal bus DB. We will not consider the specific circuit design, even though the approach used has made it possible to achieve a very high density. Whether a given memory location is interpreted as a high or low state is determined by a single process mask. There exists software which will create the required process mask for a given user program.

Internal and External RWM [Read-Write Memory] Data Storage

The scratchpad memory of the 8048 has a capacity of 64 bytes. The current address of some register is contained in the MAR register [memory address register], which has 6 bits. This 6-bit address is generated in various ways. In direct addressing, in which the opcode contains the 3-bit code for one of the 8 directly addressable registers, the address bits which are lacking are automatically made up to the full 6. As Fig. 2 shows, there are two groups of 8 directly addressable [i.e., scratchpad] registers. Which group is actually directly addressable depends on the setting of flag BS. The state of BS is controlled by program instructions for selection of

the register bank (SEL RB0 and SEL RB1). When the state of BS is low, the content of register MAR is 000rrr, while when BS is high, the content of MAR is 011rrr. The address of the directly addressable register is always set, regardless of the instruction, at the time when the opcode is read into the instruction register IR. Writing into the instruction register and MAR is controlled by the signal GDI.

In the case of instructions involving indirect addressing, what is actually performed is direct addressing, which may, however, address only register R0 or R1 (or R0' or R1'). When the opcode of an instruction with indirect data addressing is written in [the instruction register], the address 00000r or 01100r is written into MAR. The content of the register thus addressed appears at the output of the internal data memory. The signal GINAD writes the state of the memory output in memory address register MAR, losing the two highest-order bits. The new content of MAR addresses the entire internal data memory. This means that register R0 (or R1 or R0' or R1') may be addressed in isolation.

There is a 16-byte gap between the two groups of directly addressable registers. Addressing in this space is controlled by register MAR, whose content is set by the signal GSPA in accordance with the state of the stack pointer SP. While the content of the stack pointer consists of only 3 bits (8 possible addresses), the space in question has twice that capacity; each value of the SP corresponds to two memory locations. Each pair of registers represents one stack level, which holds the content of the program counter PC and the part of the status word designated PSWH. The stack pointer SP always indicates the vacant level. When the stack pointer is being used, the address register MAR always indicates the lower byte of the stack level in question. The higher byte is added to the address at the proper time by the control unit, directly acting upon the RWM [read-write memory] address decoder. The stack structure, the data storage method and the relation between the contents of the stack pointer and the register which is addressed are shown clearly in Fig. 4. Suppose, for example, that three stack levels are occupied. Then SP contains the value 011. When there is another subroutine call, a signal GSPA causes the contents 001110 to be written into MAR; this is then modified to 001111 by the control unit at a specific time. It must also be borne in mind that the registers which normally make up the stack are also accessible by instructions using indirect addressing. There is no hardware for protecting their contents from undesired overwriting or from stack overflow (i.e., of the 8 permitted levels of subroutine nesting).

Data is written into internal data memory during activation of the signal GDBM, which writes the current state of internal bus DB into the memory location. When the content of the memory location is being read, the output of RWM memory is fed to the internal bus by the signal WMDB.

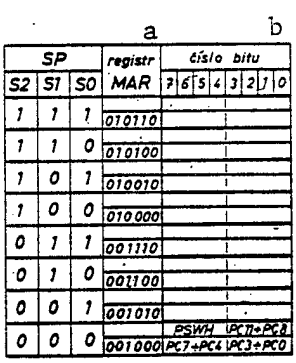


Fig. 4. Allocation and Addressing of Stack Levels

Key:

a. MAR register

b. Bit numbers

The internal data memory may be expanded by adding external RWM memory; the 8048 instruction set contains special instructions with indirect addressing for this purpose. The initial phase of selection of an indirectly addressed register in external RWM memory proceeds as in the case of internal memory. To the internal memory output is fed the content of one of registers R0, R1, R0' or R1'. Instead of signal GINAD, the signals WMDB and GDBD are generated, resulting in transfer of the content of one of the registers to the output buffer of channel 0 (OBD0). Since connection of the external data memory to the 8048 requires the same conditions as must be met for connection with external program memory, i.e., creation of data, address and control buses, the signal ALE is used in similar fashion to store the addresses of locations in RWM external memory in the same or different auxiliary buffer, which addresses one of 256 possible memory locations (all 8 bits of registers R0 or R1 are used for addressing). Depending on whether data are to be written into external memory or read from it, the 8048 generates the signal WRN or RDN. In writing, the content of accumulator ACC is first written via the ALU and the internal bus DB into the input buffer of channel 0 (OBD0), where it overwrites a no-longer-valid memory address; then the signal WRN causes the actual writing into external RWM memory.

When reading the contents of the addressed location in external RWM memory, an RDN signal obtains the contents on data bus D7-D0 and then at the input of internal bus driver BDB0. When the signals WDDB, GDBAH and GDBAL are activated, the transmission to accumulator ACC is performed via internal bus DB.

This method allows simple expansion of the total data storage capacity of to 64 + 256 = 320 bytes. While it is theoretically possible to expand it further, the circuit design and software would be too complicated. In addition, we must not let ourselves be misled by the fact that the addresses of internal and external RWM memory seem to overlap. Instructions with indirect addressing in data storage are for only internal or only external storage, and hardware is provided to prevent their exchange, even at the same addresses. This is shown schematically in Fig. 5.

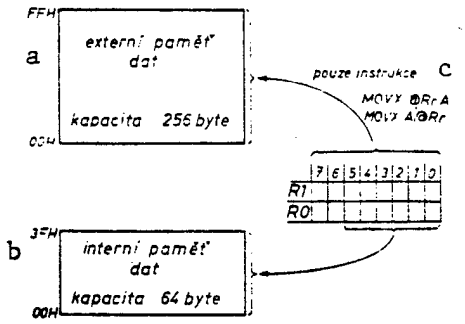


Fig. 5. Addressing of External and Internal Data Memory in 8048

Key:

a. External data memory, capacity 256 bytes
b. Internal data memory, capacity 64 bytes
c. Only instructions MOVX @Rr, A and MOVX A, @Rr

The Counter/Timer

The 8048 contains an 8-bit counter CT whose input can be connected to a source of time-discrete signals or to the TEST1 circuit. The time-discrete signal is extracted unambiguously from the oscillator frequency. For example, when the oscillator frequency is 6 MHz, the content of the counter will be incremented with a frequency of 12.5 kHz (6 MHz : 3 : 5 : 32 = 12.5 kHz). If the input is connected to the output of TEST1, the content of counter CT is incremented every time the incoming signal changes from high to low.

The counter/timer can be reset only by an instruction which sets its content in accordance with the content of ACC. The counter-timer may count to a maximum value of 0FFH; if it exceeds this value it is cleared and the CT overflow flag is set. Counter overflow also generates a program interrupt request, but only if an interrupt is enabled at that time in the processing of the program. The TF (timer flag) flop-flop is used as the overflow flag. The current status of TF can be tested by a conditional jump instruction which, if executed, clears TF. The processing of an interrupt request from counter CT is described in a separate section.

The ability to set the initial content of CT means that we can determine how many times it may increment before it overflows. In timing, we actually set an interval whose beginning is specified by execution of the sequence of instructions:

```
MOV A, TSTART
MOV T, A
EN TCNTI
STRT T
```

The first instruction loads the program constant designated by the symbol TSTART into the accumulator. The second instruction moves the contents of

accumulator ACC to the counter CT as its initial state. The third instruction allows an interrupt as a result of counter overflow. The last instruction initiates the counting process by defining the state of the 32X divider (clearing) at the start time. The end of the interval is indicated by the generation of the interrupt request. This makes it possible to create time intervals ranging from 80 microseconds to 20.48 ms. Shorter intervals can be created only by activating the timer as an event counter and feeding the output of an external divider controlled by the FV signal (accessible at the TEST0 pin) or the ALE signal to the test TEST1 input. We must, of course, meet the condition that the minimum distance between two active edges at the TEST1 input is 7.5 microseconds and the high state of the input signal lasts at least 500 ns (one entire clock period T).

Additional capabilities of the counting process result from the instruction to stop counting or transfer the content of counter CT to accumulator ACC. It is then possible to select a larger time interval of practically arbitrary length by means of software.

In the actual incrementing of the counter in the 8048, the current state of counter CT is transferred to buffer INCB by signal GCT at a suitable time. When the conditions for incrementation are met, the content of the counter, increased by 1, is fed to internal bus DB at the time of activation of the signal WPCLDB. The state of bus DB is simultaneously sampled by signal GDBCT. If the conditions for incrementing the counter are not met, its initial content is transmitted. Flag TF is set if there is a transfer from the incrementation block.

Inputs and Outputs of the 8048

The 8048 microcomputer has a total of 27 circuits for input or output of data. The states of pins TEST0, TEST1 and INTN can be tested by program branch instructions, and the other pins form three 8-bit input or output channels. Since the characteristic of these channels has a direct effect on the user characteristics of the 8048, we will discuss them in some detail. We will use a method based on description of the characteristics of the 8080A microprocessor [5]. We will also call attention to any exceptions and to a typical method of using the control signals generated by the control unit, which in Fig. 2 are shown in symbolic form next to the blocks which they control. We shall also use Table 3, which shows the waveforms and basic characteristics of the control signals.

Channel 0

The functional characteristics of channel 0 allow it to be connected to the external system bus. The circuitry is shown in Fig. 6. The state of the internal bus DB can be written in output buffer OBD0 by signal GDBD. Buffer OBD0 is a 1-bit dynamic register into which we can record new information during the time when FS is zero, which is the case, as Table 3 shows. Pins D7-D0 are controlled by the state of input buffer OBD0 only if signal TSBD is low. If TSBD is high, pins D7-D0 are in the third state and it can be connected to the data source. The incoming data are not stored in any

input buffer and therefore the designation BDBO in Fig. 2 includes several inverters and a gate with an open collector controlled by signal WDDB. Obviously the input data cannot be changed before signal WDDB is activated. In some instructions the input from channel 0 consists of data in output buffer OBDO. The connecting of this input data source requires that the signal GWD be low.

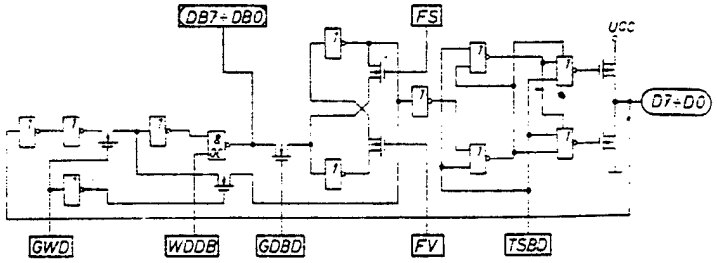


Fig. 6. Design of Channel 0 in 8048 Microcomputer

In analyzing the conditions for connection of external program or data memory, we assumed that channel 0 transmits the address or part of it on the external bus and that the channel is used to transmit the contents of the addressed memory locations. If the address was to be transmitted, we required that output buffer OBDO be freed up by transfer of its contents to the proper external buffer by means of signal ALE (at the trailing edge). According to Table 3 the basic condition, i.e., that the signal which controls writing into buffer OBDO always precedes the active edge of signal ALE, and also the condition that in this case the third state of outputs D7-DO is disabled by having signal TSBD be low, are met. The content of the addressed location in program memory is fed to the external data bus by setting signal PSENN low. To avoid conflicts on the external bus, signal TSBD must go high to keep pins D7-DO in the third state during the entire time that signal PSENN is active. The state of the external data bus is written onto the internal bus DB by signal WDDB; this should occur only when the external bus is controlled by some data source (PSENN low or RDN low) and the third state of pins D7-DO is set by signal TSBD being high. In some special instructions, the signal GWD is also used; otherwise it is constantly high. When signal GWD is as shown in Table 3, we see that the conditions are unchanged as regards reading of instructions from the external program memory.

When we operate the 8048 without a requirement for an external bus, channel 0 can be used as a static input or output. There are special instructions for this purpose (INS A, BUS, and OUTL, BUS, A), which cannot, of course, be used in alternation within a single user program. We either use all of channel 0 as an input during execution of the program and can transfer the state at output D7-DO to accumulator ACC at some time by means of the instruction INS, or we use it as an output, i.e., we constantly disable the possibility of producing a third state by setting signal TSBD low. The instructions INS and OUTL are executed by means of signals WRN and RDN, but their practical employment depends on the user. Neither of

these instructions can be used if the microcomputer is operating with the ROM external program memory. In the case when pins D7-D0 are connected to an external bidirectional bus, there is the limitation that they are in the third state when active data transmission is not in progress.

Channels 1 and 2

Both I/O channels are implemented in the same way, as shown in Fig. 7. The interconnections shown apply unchanged for the lower half of channel 2, which in addition to its basic data input and output function also performs a special function during addressing of ROM external program memory or can be connected to a type 8243 expander. A simple comparison of Figs 6 and 7 shows that the output buffers (OBD1, OBD2L and OBD2H) have almost the same design as in channel 0. The only basic difference is that during initialization of the microcomputer (RESETN signal low), they are pulled high. The same result is produced by activation of signal G1P2L, which is used only with output buffer OBD2L. The connection of the sections symbolically designated BDB1, BDB2L and BDB2H is completely identical for all channels. The only possible differences are in the control signals, but these differences are shown in Fig. 2. In the case of channel 2L, a logical switch is connected between output buffer OBD2L and the output transmitter, allowing the contents of program counter PCH to be transmitted when signal GPCHP2L is active at pins P23-P20. It is readily apparent from Table 3 that during addressing of the external program memory the contents of counter PCH are in fact fed to pins P23-P20. Correct functioning of the output transmitter requires that signal W1P2L be low during the entire time that signal GPCHP2L is active. The shape of this signal is not presented in Table 3, because it is uniquely related to the shape of the control signal waveform which writes the state of internal bus DB in the channel's output buffer (GDBP2L → OBD2L, GDBP2H → OBD2H, GDBP1 → OBD1).

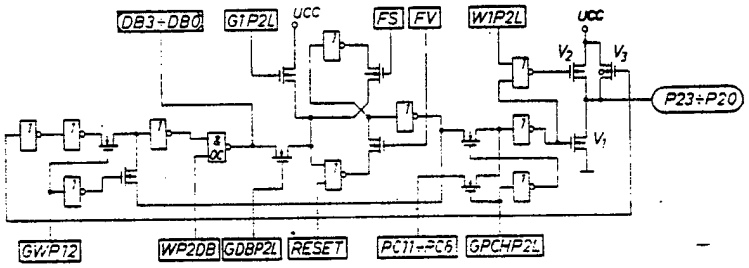


Fig. 7. Design of Channel 2L in 8048 Microcomputer

Now let us concentrate on the case in which the output amplifier is connected to the input buffer of the channel. We see that the pins of the channel constantly follow the state contained in the output buffers. Since there is no third state, the question arises how the channel will behave if we want to read data. To answer the question we must recall that the output amplifier consists of 3 transistors. Transistor V3 operates in the depletion mode and its channel is constantly conductive. Thus it presents a resistance of about 50 kohm, which forces the channel output high with a

logical gain sufficient to control the input of a TTL integrated circuit. At the same time, it is a sufficiently large resistance to the input channel pin to be controlled by a TTL gate at the low level. Transistor V2 is intended to produce good dynamic characteristics at the transition L → H; its typical impedance is about 5 kohm. This is used only if a high state is entered into the channel's input buffer. Then the gate of transistor V1 is in the low state and a signal of the type W1P2L is produced whenever it is written in the buffer of channel 1 or 2. Its duration is limited to one period T (about 500 ns). Of course, if the output buffer of the channel is low, the gate of transistor V1 is high, which makes it conductive with an impedance of about 3 kohm and also makes it impossible for transistor V2 to be opened by a signal of type W1P2L. Conductive transistor V1 sets the output of channel 1 or 2 low, and it cannot be changed by the output of a TTL gate. Therefore we may write data into the microcomputer only through the bits of channels 1 or 2 whose output buffers are in the high state during the reading of data. The source of the input signals (data) may be changed only after the end of the read signal WP1DB (WP2DB).

This behavior of channels 1 and 2 allows individual bits to be programmed for the input and output functions. For example, when the 8048 sets buffer OBD1 in state OF3H = 11110011, the external output logically connected to pins P17-P12 can change the state at pins of channel 1 only to 0073H = 01110011, i.e., it cannot cause P12 to go high. We recall that when the signal RESETN is low, it sets the state OFFH = 11111111 in the output buffers of channels 1 and 2, thus setting all bits of these channels in the input mode. According to Fig. 7, signal G1P2L also sets buffer OBD2L in the state OFH = 1111. This is used when processing instructions which control transfer of data between the 8048 and the 8243 expander. Before we examine these instructions, we refer to signal G1P2L and also understand why the setting of pins P23-P20 for the input function is performed by hardware.

The Status Word PSW of the 8048

The status word of the 8048 is generated during execution of the instruction (MOV A, PSW), which allows its contents to be loaded into the accumulator ACC. The content of the individual bits in the status word PSW is shown in Fig. 8. It is transmitted on internal bus DB when signal WSWDB is active; this signal transfers the state of carry flag CY, auxiliary carry flag AC, hardware flag F0 and flag BS, which holds information on which internal data memory registers are directly addressable at the moment, to the proper lines of bus DB. Another part of the content of PSW is written on the internal bus by signal WSPDB, which is the current value of the stack pointer SP. Simply by processing the status work, the programmer can determine how many stack levels are actually being used; this may, for example, be used in the subsequent course of the program to enable or disable processing of an interrupt request.

The part of the status word designated PSWH maintains continuity in program execution during subroutine calls. It is contained in the stack at the location shown in Fig. 4. On exiting from a subroutine the contents of CY, AC, F0 and BS may, but need not, be set in accordance with the content of

PSWH: this depends on whether the return instruction RET or RETR is used. Only instruction RETR activates the signal GDBSW, which writes the state of bus DB defined by the content of PSWH into the relevant flags.

PSW							
PSWH							
7	6	5	4	3	2	1	0
CY	AC	F0	BS	1	S2	S1	S0

Fig. 8. Status Word PSW in 8048

The 8048 Control Word CW

During program execution by the 8048, certain internal and external states can be achieved by conditional branch instructions. In essence this uses the ability of the 8048 hardware to test the individual bits of accumulator ACC. When we want to know whether accumulator bit ACC4 is high, the control unit sets the contents of temporary register TMP to state 10H by means of the constant generator and sets the ALU for the logical function AND. The output of the ALU can be schematized as follows:

TMP	0	0	0	1	0	0	0	0
ACT	X	X	X	?	X	X	X	X
ALU	0	0	0	?	0	0	0	0

By masking the nonrelevant bits in temporary accumulator ACT we can perform any type of testing of single-bit information. Depending on the contents of the selected bit in the accumulator, during transfer to internal bus DB the output of the ALU sets a state which can be unambiguously distinguished. The state of the internal bus may be either zero or not zero; the conditional jump testing unit determines which. Whether the output of this unit is accepted by the control unit, and whether a zero or nonzero content of the bus is considered to be a positive result, depends on the type of instruction being executed (fourth bit of instruction opcode).

If we transfer the contents of accumulator ACC to temporary accumulator ACT by means of suitably organized instructions, we can again use this mechanism for testing the content of individual bits. For this purpose, during execution of the conditional jump instruction the 8048 generates the control word CW whose structure is shown in Fig. 9. Activation of signal WCWDB causes the content of internal bus DB to be set in accordance with the current state of the carry flag CY, the state of software flags F0 and F1, the state of external pins INTN, TEST0 and TEST1, and the state of flag TF, which monitors overflow of counter CT. Now it is only necessary to activate signals GDBTAH and GDBTAL, and the content of control word CW is entered into temporary accumulator ACT rather than accumulator ACC. The individual bits are processed by the method described above, except that the control unit generates a different sequence of signals. This will all become clear when we describe the processing of specific instructions below in tabular form.

CW							
7	6	5	4	3	2	1	0
CY	1	F0	INT	F1	TEST1	TEST 0	TF

Fig. 9. Control Word CW of 8048

Flags F0 and F1

The states of flags F0 and F1 can be changed by suitable instructions during program execution. They are used by the programmer to branch the program in accordance with the states of auxiliary variables.

The Control Unit

The main function of the control unit is to create the conditions for correct operation of the 8048 during all possible functional modes. The simplest to describe of these is instruction execution; we have all of the basic knowledge needed for the purpose. We know the operating principles of the individual components of the 8048, the significance of the control signals, and the possible times of their generation (Table 3). If in addition we define, as in Table 5, a list of symbols used for an abbreviated description of the 8048, we have everything we need to provide the future user of the microcomputer with complete information on the execution of all instructions. Therefore we trust that the information brought together in Table 6 is intelligible and complete.

Table 5. Symbols Used in Abbreviated Description of Functioning of 8048

a Symbol		b Význam symbolu	c Příklad
⟨ ⟩	d	1. nebo 2. byte instrukce nebo několik bitů op. kódu instrukce	*⟨B2⟩, ⟨B1. 2—0⟩*
( )	e	obsah paměťového místa	*(ACC), (CY), (SP)*
[( )]	f	obsah paměti nepřímo adresovaný	*[(MAR)]*
Rr	g	označení přímo adresovaného registru	*ADD A, Rr*
@ Rr	h	označení nepřímo adresovaného registru	*MOV @ Rr, A*
# data	i	programová konstanta	*ORL BUS, # data*
addr	j	2. byte instrukce; který se ukládá do nižší části čítače programu *PCL*	*JFO addr*
BUS	k	označení kanálu *0*	*OUTL BUS, A*
Pp	l	označení kanálu *1* nebo	*(ACC) ← (Pp)*
(aaa)	m	část operačního kódu instrukce, která určuje přístí obsah bitů *PC10* až *PC8*	*(aaa10100)*
(rrr)	n	část operačního kódu instrukce, která obsahuje adresu přímo adresovaného registru	*(01101rrr),*
Kb	o	konstanta, která určuje, který bit střádače *ACC* bude testován na úroveň H	*(TMP) ← Kb*
K	p	hodnota konstant generovaná generátorem konstant *(tabulka 4)*	*(TMP) ← K*
MOD	q	část operačního kódu instrukce, která určuje činnosti expandéru 8243	*(OBD2L) ← MOD*

[Table 5 continued on following page]

Ppe	r	kanál expandéru 8243		*ORLD Ppe, A*
L	s	označení bitů *3* až *0*		*(ACCL), (DBL)*
H	t	označení bitů *7* až *4*		*(ACCH), (+H)*
(+)	u	aritmetický součet	x výstup bloku *ALU*	*(ACC) ← (+)*
(∨)	v	logický součin		*(DB) ← (∨)*
(∧)	w	logický součet		*(ACC) ← (∧)*
(⊕)		EXCLUSIVE OR		*(ACC) ← (⊕)*
(RT)	y	rotace doprava		*(ACC) ← (RT)*
(+C)	z	výstup bloku *ALU* určen aritmetickým součtem vstupních operandů a přenosu		*(ACC) ← (+C)*
C	A	přenos		*'CY) ← C*
TEST(DB)	B	test nulového obsahu interní sběrnice *DB*		*DB) ← (+) TEST(DB)*
←	C	přiřazovací příkaz		*(TMP) ← 00H*
↔	D	výměna obsahů		*(ACC) ↔ (Rr)*
×	E	pokud je podmínka skoku splněna, zvětšená hodnota čítače programu *PCL* se ztratí		*× IF FALSE (PC) ← (PC) + 1*
× ×.	F	externí paměť dat		

Key:

a. Symbol
b. Meaning
c. Example
d. First or second byte of instruction or several bits of instruction opcode
e. Contents of memory location
f. Contents of indirectly addressed memory
g. Name of directly addressed [general-purpose] register
h. Name of indirectly addressed [scratchpad] register
i. Program constant
j. Second byte of instruction, stored in lower half of program counter PCL
k. Channel 0
1. Channel 1 or [2]
m. The part of the opcode which gives the next value of bits PC10-PC8
n. The part of the opcode which contains the address of a directly addressed register
o. A constant indicating which bit of accumulator ACC is to be tested for a logical 1
p. The value of constant generated by constant generator (Table 4)
q. The part of the opcode which determines the function of expander 8243
r. Channel of 8243 expander
s. Bits 3-0
t. Bits 7-4
u. Arithmetic sum
v. Logical product
w. Logical sum
x. ALU outputs
y. Right rotation
z. Output of ALU block resulting from arithmetic addition of output operands and carry
A. Carry
B. Test for zero on internal bus DB
C. Assignment statement
D. Swap of contents
E. If jump condition is fulfilled, incremented value of program counter PCL is lost
F. External data memory

CLRC	27	NULOVANI CY	(CY)←0H	*		10010111					(CY)←0						
CPLC	28	DOPLNEK CY	(CY)←NOT(CY)	*		10100111					(CY)←(CYN)						
CLRFØ	29	NULOVANI F0	(F0)←0H			10000101					(F0)←0						
CPLFØ	30	DOPLNEK F0	(F0)←NOT(F0)			10010101					(F0)←(F0N)						
CLRF1	31	NULOVANI F1	(F1)←0H			10100101					(F1)←0						
CPLF1	32	DOPLNEK F1	(F1)←NOT(F1)			10110101					(F1)←(F1N)						
INC Rr	33	PRICTENI 1 K PRIMO ADR. REGISTRU	(Rr)←(Rr)+1 r = 0÷7			00011rrr				(ACT)←[(MAR)] (TMP)←01H		[(MAR)]←(+)					
INC @R	34	PRICTENI 1 K NEPRIMO ADR. REGISTRU	[(Rr)]←[(Rr)]+1 r = 0,1			0001000r			(MAR)←[(MAR)]	(ACT)←[(MAR)] (TMP)←01H		[(MAR)]←(+)					
DEC Rr	35	ODECTENI 1 OD PRIMO ADR. REGISTRU	(Rr)←(Rr)−1 r = 0÷7			11001rrr				(ACT)←[(MAR)] (TMP)←FFH		[(MAR)]←(+)					
MOV A,Rr	36	PRESUN PRIMO ADRES. REGISTRU DO STRADACE	(ACC)←(Rr) r = 0÷7			11111rrr				(TMP)←00H (ACT)←[(MAR)]		(ACC)←(+)					
MOV A,@Rr	37	PRESUN NEPRIMO ADRES. REGISTRU DO STRADACE	(ACC)←[(Rr)] r = 0,1			1111000r			(MAR)←[(MAR)]	(ACT)←[(MAR)] (TMP)←00H		(ACC)←(+)					
MOV A,#data	38	PRESUN KONSTANTY DO STRADACE	(ACC)←(B2)			00100011	*						(ACC)←(B2)		(PC)←(PC)+1		
MOV Rr,A	39	PRESUN STRADACE DO PRIMO ADRES. REGISTRU	(Rr)←(ACC) r = 0÷7			10101rrr				(TMP)←00H		[(MAR)]←(+)					
MOV @Rr,A	40	PRESUN STRADACE DO NEPRIMO ADRES. REGISTRU	[(Rr)]←(ACC) r = 0,1			1010000r			(MAR)←[(MAR)]	(TMP)←00H		[(MAR)]←(+)					
MOV Rr,#data	41	PRESUN KONSTANTY DO PRIMO ADRES. REGISTRU	(Rr)←(B2)			10111rrr	*						[(MAR)]←(B2)		(PC)←(PC)+1		
MOV @Rr,#data	42	PRESUN KONSTANTY DO NEPRIMO ADRES. REGISTRU	[(Rr)]←(B2) r = 0,1			1011000r	*		(MAR)←[(MAR)]				[(MAR)]←(B2)		(PC)←(PC)+1		
MOV A,PSW	43	NAPLNENI STRADACE STAVOVYM SLOVEM	(ACC)←(PSW)			11000111				(ACT)←(PSW) (TMP)←00H		(ACC)←(+)					
MOV PSW,A	44	NASTAVENI STAVOVEHO SLOVA OBSAHEM STRADACE	(PSW)←(ACC)	*	*	11010111				(TMP)←00H		(PSW)←(+)					
XCH A,Rr	45	VYMENA STRADACE A PRIMO ADRES. REGISTRU	(ACC)↔(Rr) r = 0÷7			00101rrr				(ACC)←[(MAR)] (TMP)←00H		[(MAR)]←(+)					
XCH A,@Rr	46	VYMENA STRADACE A NEPRIMO ADRES. REGISTRU	(ACC)↔[(Rr)] r = 0,1			0010000r			(MAR)←[(MAR)]	(ACC)←[(MAR)] (TMP)←00H		[(MAR)]←(+)					
XCHD A,@Rr	47	VYMENA STRADACE A NEPRIMO ADRES. REGISTRU PRO BITY 3÷0	(ACCL)↔[(Rr)]L r = 0,1			0011000r			(MAR)←[(MAR)]	(TMP)←00H (ACCL)←[(MAR)] (ACTH)←[(MAR)]		[(MAR)]←(+)					
MOVX A,@Rr	48	NAPLNENI STRADACE EXTERNI PAMETI DAT	(ACC)←[(Rr)]XX r = 0,1			1000000r				(OBDO)←[(MAR)]				(ACC)←(BOBO)			
MOVX @Rr,A	49	PRESUN STRADACE DO EXTERNI PAMETI DAT	[(Rr)]XX←(ACC) r = 0,1			1001000r				(OBDO)←[(MAR)] (TMP)←00H		(OBDO)←(+)					
MOVP A,@A	50	PRENOS DAT Z PAMETI ROM DO STRADACE NA DANE STRANCE	(PCL)←(ACC) (ACC)←[(PC)]			10100011				(TMP)←00H (PCL)←(+)			(ACC)←[(PC)]		OBNOVENI PC		
MOVP3 A,@A	51	PRENOS DAT Z PAMETI ROM DO STRADACE NA STRANCE 3	(PCL)←(ACC) (PC10÷8)←011 (ACC)←[(PC)]			11100011		↓	↓	(TMP)←00H (PCL)←(+) PC10÷8←011	↓		(ACC)←[(PC)]		OBNOVENI PC		

[Table 6 continued on following page]

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MOV A,T 77	OBSAH CITACE SE PRENESE DO STRADACE	(ACC)←(CT)			01000010						(ACC)←(CT)						
MOV T,A 78	OBSAH STRADACE SE PRENESE DO CITACE	(CT)←(ACC)			01100010					(TMP)←00H		(CT)←(+)					
STRT T 79	START CITACE CASU				01010101					100	DELIC ÷32 VYNULOVAN	START T					
STRT CNT 80	START CITACE UDALOSTI				01000101							START CNT					
STOP CNT 81	STOP CITACE				01100101							STOP CT					
EN TCNTI 82	POVOLENI PRERUSENI OD CITACE				00100101					75 POVOLENI							
DIS TCNTI 83	ZAKAZANI PRERUSENI OD CITACE				00110101					76 ZAKAZANI							
CALL addr 84	VOLANI PODPROGRAMU	[(SP)]←(PC),PSWH (PC8÷10)←(aaa) (SP)←(SP)+1 (PCL)←(B2) (PC11)←(DBF)			aaa10100	*				(TMP)←00H	(MAR)←(SP)	(ACTL)←(PCH) (ACTH)←(PSWH)	(PCL)←(B2)	(PCH)←(IR7-5) (PC11)←(DBF)	[(MAR)]←(PCL)+1	[(MAR)+1]←(+C) (SP)←(SP)+1	
RET 85	NAVRAT Z PODPROGRAMU BEZ OBNOVENI PRIZNAKU	(SP)←(SP)−1 (PC)←[(SP)]			10000011						(SP)←(SP)−1 (MAR)←(SP)	(PCH)←[(MAR)+1]	(PCL)←[(MAR)]				
RETR 86	NAVRAT Z PODPROGRAMU Z OBNOVENIM PRIZNAKU	(SP)←(SP)−1 (PC)←[(SP)] 101 OBNOVENI PSWH	*	*	10010011						(SP)←(SP)−1 (MAR)←(SP)	(PCH)← (PSWH)← [(MAR)+1]	(PCL)←[(MAR)]				
IN A,Pp 87	NAPLNENI STRADACE DATY ZE VSTUPU KANALU 1 NEBO 2	(ACC)←(P_p) P=1,2			000010pp									(ACC)←(BDBp)			
OUTL Pp,A 88	PRESUN STRADACE DO VYSTUPNI PAMETI KANALU 1 NEBO 2	(P_p)←(ACC) P=1,2			001110pp					(TMP)←00H		(OBDp)←(+)					
ANL Pp,#data 89	LOGICKY SOUCIN DAT VE VYST. PAMETI KANALU 1 NEBO 2 A KONSTANTY	(P_p)←(P_p) AND (B2) P=1,2			100110pp	*						(ACT)←(OBDp)	(TMP)←(B2)		(PC)←(PC)+1	(OBDp)←(∧)	
ORL Pp,#data 90	LOGICKY SOUCET DAT VE VYST. PAMETI KANALU 1 NEBO 2 A KONSTANTY	(P_p)←(P_p) OR (B2) P=1,2			100010pp	*						(ACT)←(OBDp)	(TMP)←(B2)		(PC)←(PC)+1	(OBDp)←(V)	
INS A,BUS 91	NAPLNENI STRADACE DATY ZE VSTUPU KANALU 0	(ACC)←(BUS)			00001000									(ACC)←(BDB0)			
OUTL BUS,A 92	PRESUN STRADACE DO VYSTUPNI PAMETI KANALU 0	(BUS)←(ACC)			00000010					(TMP)←00H		(OBD0)←(+)					
ANL BUS,#data 93	LOGICKY SOUCIN DAT VE VYST. PAMETI KANALU 0 A KONSTANTY	(BUS)←(BUS) AND (B2)			10011000	*						(ACT)←(OBD0)	(TMP)←(B2)		(PC)←(PC)+1	(OBD0)←(∧)	
ORL BUS,#data 94	LOGICKY SOUCET DAT VE VYST. PAMETI KANALU 0 A KONSTANTY	(BUS)←(BUS) OR (B2)			10001000	*						(ACT)←(OBD0)	(TMP)←(B2)		(PC)←(PC)+1	(OBD0)←(V)	
MOVD A,P_{PE} 95	PRESUN DAT Z EXPANDERU 8243 DO STRADACE	(ACCL)←(P_{PE}) (ACCH)←0H PE=4÷7			000011pp					(OBD2L)←M00				(ACCL)←(BDB2L) (ACCH)←0H			
MOVD P_{PE},A 96	PRESUN DAT ZE STRADAC DO EXPANDERU 8243	(P_{PE})←(ACCL) PE=4÷7			001111pp					(TMP)←00H (OBD2L)←M00		(OBD2L)←(+L)					
ANLD P_{PE},A 97	LOGICKY SOUCIN DAT EXPANDERU 8243 A STRADACE	(P_{PE})←(P_{PE}) AND (ACCL) PE=4÷7			100111pp					(TMP)←00H (OBD2L)←M00		(OBD2L)←(+L)					
ORLD P_{PE},A 98	LOGICKY SOUCET DAT EXPANDERU 8243 A STRADACE	(P_{PE})←(P_{PE}) OR (ACCL) PE=4÷7			100011pp					(TMP)←00H (OBD2L)←M00		(OBD2L)←(+L)					
NOP 99	PRAZDNA OPERACE				00000000												

[Key to Table 6 on following page]

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Key:

a. Instruction
b. Cycle
c. Name
d. Description
e. Function
f. Opcode

1. Add contents of directly addressed register to accumulator
2. Add contents of indirectly addressed register to accumulator
3. Add constant to accumulator
4. Add contents of directly addressed register and carry to accumulator
5. Add contents of indirectly addressed register and carry to accumulator
6. Add constant and carry to accumulator
7. AND contents of directly addressed accumulator with accumulator
8. AND contents of indirectly addressed accumulator with accumulator
9. AND constant with accumulator
10. OR directly addressed register with accumulator
11. OR indirectly addressed register with accumulator
12. OR constant with accumulator
13. Exclusive OR contents of directly addressed register with accumulator
14. Exclusive OR contents of indirectly addressed register with accumulator
15. Exclusive OR constant with accumulator
16. Increment accumulator by 1
17. Decrement accumulator by 1
18. Clear accumulator
19. Complement accumulator
20. Convert accumulator to binary coded decimal
21. Swap accumulator halves
22. Rotate accumulator left
23. Rotate accumulator left through carry
24. Rotate accumulator right
25. Rotate accumulator right through carry
26. In BCD [binary coded decimal]
27. Clear CY
28. Complement CY
29. Clear F0
30. Complement F0
31. Clear F1
32. Clear F1 Complement F1
33. Increment directly addressed register by 1
34. Increment indirectly addressed register by 1
35. Decrement directly addressed register by 1
36. Move contents of directly addressed register to accumulator
37. Move contents of indirectly addressed register to accumulator
38. Move constant to accumulator
39. Move contents of accumulator to directly addressed register
40. Move contents of accumulator to indirectly addressed register
41. Move constant to directly addressed register
42. Move constant to indirectly addressed register

43. Move status word to accumulator
44. Move contents of accumulator to status word
45. Swap contents of accumulator and directly addressed register
46. Swap contents of accumulator and indirectly addressed register
47. Exchange bits 3-0 of accumulator and directly addressed register
48. Load contents of external data memory byte into accumulator
49. Load contents of accumulator into external data memory byte
50. Move data from ROM memory to accumulator on page specified
51. Transfer data from ROM memory to accumulator on page 3
52. External interrupt enable
53. External interrupt disable
54. Select bank 0 of directly addressed registers
55. Select bank 1 of directly addressed registers
56. Select bank 0 of program memory
57. Select bank 1 of program memory
58. Enable internal clock input at TEST0
59. Unconditional jump
60. Indirect jump
61. Decrement directly addressable register by 1 and jump if contents differ from 0
62. Jump if CY = H
63. Jump if CY = L
64. Jump if ACC = 00H
65. Jump if ACC $\neq$ 00H
66. Jump if TEST0 = H
67. Jump if TEST0 = L
68. Jump if TEST1 = H
69. Jump if TEST1 = L
70. Jump if F0 = H
71. Jump if F1 = H
72. Jump if TF = H
73. Jump if ININ = L
74. Jump if accumulator but ACC_n = H
75. Enable
76. Disable
77. Transfer contents of counter to accumulator
78. Transfer contents of accumulator to counter
79. Start clock
80. Start event counter
81. Stop counter
82. Counter interrupt enable
83. Counter interrupt disable
84. Call subroutine
85. Return from subroutine without restoring stack pointer
86. Return from subroutine and restore stack pointer
87. Load data from input ports 1 or 2 into accumulator
88. Load contents of accumulator into output buffer of channel 1 or 2
89. AND data in channel 1 or 2 buffer with constant
90. OR data in output channel buffer 1 or 2 with constant
91. Load data from input port 0 into channel
92. Move accumulator contents into output buffer of channel 0

93. AND data in output buffer of channel 0 with constant
94. OR data in output buffer of chennel 0 with constant
95. Move data from 8243 expander to accumulator
96. Move data from accumulator to 8243 expander
97. AND data from expander 8243 with accumulator
98. OR data from 8243 expander with accumulator
99. Dummy operation
100. 32X divider cleared
101. Restore PSWH

The Instruction Set of the 8048

The power of every computer system depends to a considerable degree on the scope of its instruction set and the effectiveness of the individual instructions. Evaluating a microcomputer in these terms requires considerably more practical experience than the authors currently have. Therefore we will put aside the question as to why these instructions and not others are provided; they are there simply because this microcomputer is the world standard.

The entire instruction set of the 8048 is presented in Table 6. For each instruction, designated by its mnemonic, we give a brief verbal description of the function performed and the binary opcode, and indicate whether it can activate flags CY and AC, the number of bytes in the instruction, and the number of machine cycles M required for its execution. The actual performance of the instruction during the instruction cycle is described in detail by the symbols presented in Fig. 2 and Table 5. We can examine the required control signals generated during period T in Table 3. We illustrate a possible approach to the use of this documentation through several typical examples.

First we consider the operations which the 8048 performs independently of instructions. They are controlled by the control signals marked with a 1 in Table 3. Since execution of instructions is begun by loading them into instruction register IR, we begin with the corresponding signal GDI, which is generated only in period T1 of the first machine cycle. The opcode of the instruction can be written on the internal bus from internal or external ROM program memory. In the case of internal program memory it is activated by signal WROMDB. When reading an instruction from external ROM memory, its pins are connected via the external bus to D7-D0 only if signal PSENN is low. The data is written on internal bus DB by signal WDDB. In order for us to be able to read from the program memory, the required address must be prepared in advance, i.e., during processing of the preceding instruction. The description below will show when the address of the next instruction is generated.

The signal GDI also sets the content of the address register of the internal data memory (MAR) in accordance with the content of the three lowest-order bits of the instruction opcode and the current value of flag BS. This sets the address of one of eight possible directly addressable

registers, whose contents are readied at the output of the internal data memory.

The starting operands in the ALU are set by signals GATA and GITR. The former controls writing of the contents of accumulator ACC into temporary accumulator ACT, and the latter loads state 00H into temporary register TMP. As shown in Table 4, this value is stored in the constant generator and is always addressed during clock period T1. The last-mentioned operations make it possible to obtain the contents of accumulator ACC at the ALU output in clock period T3, which is actually done only in the case of instructions RLA and RLCA, when it is necessary to load register TMP with the contents of accumulator ACC.

In clock period T2 the internal bus is reserved for transmission of the new contents of the program counter PC. Signal WPCLDB transfers to bus DB the value stored in buffer INCB, incremented by 1. It is easy to see from Table 3 that the last content of buffer INCB was determined by transfer of the contents of PCL2 (by signal GPC) during clock period T5 of the preceding instruction. The new value in program counter PCL is written at the same time into buffers PCL1 and PCL2 by signals GDBPC and GDBNPC. If the contents of counter section PCL were transferred to PCH, signal GPCH1 is also generated. We have seen that the subsequent memory location in program memory is addressed considerably in advance. At the conclusion of incrementation of the program counter PC, the current content was no longer contained in buffer INCB. Therefore the control unit generates signal GCT, which transfers the contents of counter CT into that buffer. Clock period T3 is also the period in which the internal bus DB is not occupied by instructions for independent data transfer.

During clock period T4, signal WPCLDB is again activated. The contents of buffer INCB or the contents of counter CT stored in it are transferred to the bus. If the conditions for incrementing the counter have been met, the contents of the counter, incremented by 1, are transmitted. Otherwise the original value stored in counter CT is transmitted. The new, or in most cases the unchanged, counter value is written into counter CT by signal GDBCT. When the transmission ends, buffer INCB again becomes free, and therefore signal GPC writes the contents of buffer PCL2 in it. This begins preparation of the address of the next memory location in program memory. This mechanism for alternating loading of auxiliary buffer INCB with the contents of program counter PCL and counter CT is constantly repeated in single-cycle instructions. We can use internal bus DB for the execution of the operation called for by a single-cycle instruction only in clock periods T3 and T5.

Two-byte instructions, which are automatically two-cycle instructions, are fundamentally different. Their execution must wait for the second byte, so that some operation must be delayed and transferred to a new clock period T in the second machine cycle. Therefore, the degree of functional utilization of the instruction cycle time is considerably less in most two-cycle instructions. We can see from Table 6 that there are also 1-byte instructions whose instruction execution takes two machine cycles M1 and M2.

The execution of the two-cycle instruction follows smoothly from the activity described for a single-cycle instruction. The implicit operations of the microcomputer are not changed. We note that the address of the subsequent memory location in program memory is prepared during the first cycle and that the contents of PCL are stored in buffer INCB. Of course, it will be read from program memory only if the instruction is two bytes long. Only in this case will the signal WROMDB be activated in clock cycle T1, writing the contents of the second byte from program memory on bus DB. To read from external ROM memory, signals PSENN = L and WDDB are used as already described.

It is important to bear in mind in the case of a two-cycle instruction that the current state on the internal bus DB is written into memory PCL1 by signal GDBPC and into memory PCL2 by signal GDBNPC during clock period T1, regardless of the instruction. It is evident from Table 6 that transfer does not occur in all two-cycle instructions. This means that the microcomputer now addresses a memory location in program memory whose address on the page in question specified by the contents of bus DB during clock period T1 of the second cycle.

If this instruction is two bits long, the program counter PC must again be incremented. Therefore a signal WPCLDB is generated during clock period T3 of the second cycle and transmits the contents of register INCB incremented by 1 on the bus. While this operation is always carried out, the new contents of counter PCL are transferred to buffers PCL1 and PCL2 only under specific conditions specified by the instruction to be executed (appearance of signals GDBPC and GDBNPC during clock period T3 of the second cycle). The address of the subsequent memory location in program memory is finally determined during clock period T3 of the second cycle in two-cycle instructions. Therefore, the contents of PCL2 may be written in buffer INCB by a signal GPC generated at the beginning of clock period T5, again creating the conditions for further incrementation of program counter PC. It follows from this description that nothing is done with the contents of counter CT during the second machine cycle.

We have gained a basic idea of the operations which are carried out by the microcomputer in virtually every instruction. The power of the microcomputer depends to a large degree on the usability of the internal bus DB for transmission of the data being processed. Clock periods T3 and T5 remain unused in one-cycle instructions. Two-cycle instructions enable us to use clock periods T2, T4 and T5 of the second cycle as well. We may say, with some oversimplification, that clock period T3 of the first cycle is reserved for transmission of operands to the input of the ALU, while in clock period T5 of the first cycle the output of the ALU is transmitted or the operands in registers ACT or TMP are changed. This activity is also performed in clock period T2 of the second cycle. The ALU outputs thus can be transmitted during period T4 of the second cycle. Flags CY and AC are set in period T5 regardless of the number of machine cycles.

Another feature of the 8048's functioning is typical of all instructions with indirect addressing in internal data memory. In them, a signal GINAD

is generated during period T2 of the first cycle and sets the new contents of register MAR in accordance with the state of the data memory output. The output state is determined by the content of the register whose address was written in MAR during period T1 by signal GDI (one of the directly addressable registers). Then the memory output is set in accordance with the contents of the register whose address is now in MAR.

All the conditions have now been provided for reading Table 6, for correct interpretation of the operations indicated in Fig. 2, and for precise time determination of the operations in accordance with Table 3. We must also mention the use of the table of constants. The reason that the control unit generates a constant of the specified value can be derived from the conditions for performance of the basic arithmetic and logical operations in the ALU. Details may be found in Ref. 5 or Table 4, in which typical uses of the various constants are shown, may be used for instruction.

Provided that we have at least partially understood the operations of the 8048 which are performed independently of the specific instruction, it will not be excessively difficult to understand operations directly associated with the execution of the instructions themselves. For example, we start by considering the instruction ADD A, Rr, which reads the contents of accumulator ACC and a directly addressable register in internal data memory and stores the result in accumulator ACC. We know that one operand has been prepared at the ALU output during period T1, and that the second may be transmitted as soon as the internal bus is free, i.e., during period T3. Because the contents of the register addressed are prepared at the output of the internal data memory, it suffices to activate signals WMDB and GDBTR, and the required transmission of the second operand is carried out. The status of the ALU is saved in clock period T4, and during period T5 the output of the ALU is set in accordance with the result of arithmetic addition. We can again transfer the desired result via the now available bus DB to the accumulator by activating signals WALUDB, GDBAH and GDBAL. Flags CY and AC are set at the same time. It is easy to see that replacement of the directly addressed register by an indirectly addressed register does not occur during the actual processing of the instruction. If one operand is immediate (e.g., ADD A, #data), the ALU inputs will be specified only in period T1 of the second machine cycle. Although the internal bus DB is free during the subsequent period T2, the ALU outputs are not saved. The bus is again occupied during period T3. Accordingly, the result of arithmetic addition is transmitted on the bus only in period T4. The procedure is quite similar for other instructions; only the operands differ, and the output of the ALU is determined by some arithmetic or logical function (+, $\wedge$, $\vee$, $\oplus$, RT).

Perhaps the most complex instruction in the 8048 is CALL. Together with instruction JMP it allows movement throughout the ROM program memory. The task of the CALL instruction is to set the program counter PC to the initial address of a subroutine and in addition to save the address from which the program will begin after return from the subroutine, along with section PSWH of the status word (Fig. 4).

After the opcode of the instruction CALL addr is read, the program counter PC is incremented and the second byte of the instruction is addressed. In period T3, temporary register TMP is cleared even though it has been zero since period T1. In T4, the contents of the address register MAR are set in accordance with the current value of the stack pointer SP. The transfer is controlled by signal GSPA and may be carried out during this period because the internal bus DB is not being used. We can see from Fig. 4 that register MAR addresses the lower byte of the unoccupied stack level. The first instruction cycle ends with transfer of the contents of the program counter PCH to the lower half of the temporary accumulator (ACTL) and part of the status word (PSWH), defined in Fig. 8, is written in the upper half of accumulator ACTH. These transfers are controlled by signals WPCHDB, WSWDB, GDBTAH, and GDBTAL.

The second instruction cycle writes the second byte directly into part of the program counter PCL (PCL1 and PCL2). The old value of buffer PCL2 is written into buffer INCB at the same time by signal GPC. Now the contents which are symbolically designated "aaa" in the opcode are copied from bits 7-5 of the IR output onto the bus. Another bus line indicates the current state of flag DBF (DB3 = DBF, DB2-DB0 = aaa). Signal GDBPCH is activated and the initial address of the subroutine is prepared in program counter PC. We must also store in the stack the address for continuation of the main program. The lower-order half of counter PCL, stored in buffer INCB, is incremented and written into the lower byte of the stack level in question by signals WPCLDB and GDBM. If a carry was found during transfer from buffer INCB, it must be added to the original content of the program counter PCH, which is stored in temporary accumulator ACT. Thus the required incrementation is carried out in the ALU. The upper byte of the specified stack level contains the result of arithmetic addition of the contents of the temporary accumulator ACT, the zero content of register TMP, and the carry value. The transfer is controlled by signals WALUDB and GDBM. The CALL instruction ends with incrementation of the stack pointer.

Another interesting group of instructions are the conditional jump instructions. Their characteristic feature is that they allow program jumps to be carried out only within a given page of program memory (only the value in PCL is changed). The new value of the program counter PCL forms the second byte of the instruction. As an example, let us follow the execution of the instruction JNT1 addr, where the jump is made if the input at TEST1 is low. According to Fig. 9, the value at the TEST1 input is part of the control word CW, which is written on internal bus DB during period T3 by signal WCWDB and is stored via the bus in temporary accumulator ACT by means of signals GDBTAH and GDBTAL. The content of temporary register TMP is determined by the constant generator. The signal GITR writes a constant which masks the other bits of the control word except the bit with the value of TEST1. The ALU output is determined by the AND function which is set and the value of the tested variable, TEST1. In period T5 the ALU output is fed to the internal bus but is not transferred further. The auxiliary internal control unit flop-flop is set in accordance with whether the current state of the bus is zero or nonzero. After decoding the

instruction, the control unit decides which state of the flip-flop is to be treated as affirmative for the instruction in question. Its activity is illustrated in Fig. 10. The state of signal TESTN is important for further processing of the instruction. If it is low, this means that the jump condition has been met. Actually, the execution of the instruction continues regardless of which state of TESTN is found. In period T1, the second byte of the instruction is read from ROM and stored in the lower half of the program counter PCL (PCL1, PCL2). We may again recall that the old value of program counter PCL is stored in buffer INCB, where it was moved at the beginning of the preceding period T5 by the signal GPC. We must now wait until period T3 of the second cycle, which is reserved for transmission of the incremented value of counter PCL. Of course, if the jump condition has been met (TESTN low), the control unit generates signal WPCLDB, which puts the contents of buffer INCB, incremented by 1, on bus DB but does not activate signals GDBPC and GDBNPC. If the jump condition has not been met (TESTN high), the control unit also generates signals GDBPC and GDBNPC and the contents of counters PCL1 and PCL2 are changed to the address of the instruction directly following the conditional jump instruction.

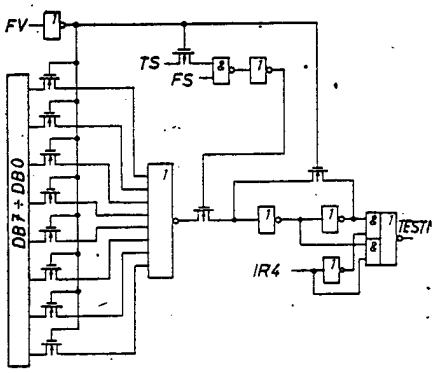

Fig. 10. Circuit for Testing for Zero on Intern Bus of 8048

To meet the condition that the conditional jump is executed only to the same page of program memory, the first part (opcode) of a jump instruction must not be located on the last address of the page.

The instructions JMPP @A, MOVP A, @A, and MOVP3 A, @A are interesting in connection with program memory. One of their characteristics is that the content of counter PCL is set in accordance with the value in accumulator ACC. This is fed to internal bus DB via the ALU, which carries out arithmetic addition of the contents of temporary accumulator ACT with the zero content of register TMP. Thus the value in the program counter PC addresses a new memory location on the same page (or on the third page), which is later written into the program counter PCL (indirect jump) or into the accumulator ACC (which is helpful in table lookup). In the case of the MOVP instructions, it is useful to bear in mind that the content of ACC has changed only the content of memory PCL1, which directly controls the ROM

memory address decoder. Therefore, in these instructions, during period T3 of the first cycle the control unit generates the signal GDBPC. In period T3 of the second cycle, under this instruction the value of buffer INCB is transferred without incrementation. The value of the counter PCL, which was reserved for the content of accumulator ACC only during the execution of the instruction, is updated. The instructions involve no jump in the value of the program counter PC, other than normal incrementation.

Finally, we will consider instructions which operate with the I/O channels. The execution of the IN and OUT instructions is rather obvious. The value which we wish to transfer to the output buffer (OBD0, OBD1, OBD2L, OBD2H) is formed at the output of the ALU by a suitable arithmetic or logical operation. The situation in reading of data is even simpler. The state of the input data fed to the pins of channel 0, 1 or 2 is sampled at bus DB in period T2 by a control signal WDDB, WP1DB, or WP2DB, and directly stored in accumulator ACC. The user program must meet the conditions which were described in more detail in the discussion of the individual channels. We merely recall that data cannot be output from channel 0, since it is operating in the static mode and only the output instruction was used (OUTL BUS, A). For channels 1 or 2, input is possible only through bits whose input buffers currently contain a 1.

When we examine the execution of instructions of the type ANL BUS, #data, we will see that signals GWD or GWP12 (period T5 of the first cycle) were used in transferring data from the various input buffers of the channels to the accumulator ACT.

If in some applications the 8048 does not have enough pins for input-output, the number can be increased in several ways:

1. Use of 8080 or 8085 series circuits. The most likely to be usable are types 8255A, 8212 and 8251 [6, 7]. Interface circuits for parallel or series communication work with the microprocessor via the external data, address, and control buses. Fig. 11 shows an example of an arrangement in which the interface circuit is addressed as a memory location in external storage. This must be borne in mind if we are considering using external data memory. Data transmission of this type can be carried out only by channel 0 with the instruction MOVX@Rr, A or MOVX A, @Rr.

2. Somewhat different possibilities for interfacing the computer to the surroundings are offered by channels 1 and 2. It is difficult to give a typical example of their use. They are used for reading the status of the keyboard, controlling a calculator display, a digital-analog or analog-digital converter or an interrupt system, or controlling or reading the states of various sensors, switches and indicators.

The wide range of uses of channels 1 and 2 runs into the problem of an insufficient number of lines with the right characteristics. Therefore the 48 series of microcomputers has been supplemented with a highly specialized circuit which makes it possible to expand the number of leads on the microcomputer that can be used for data input and output.

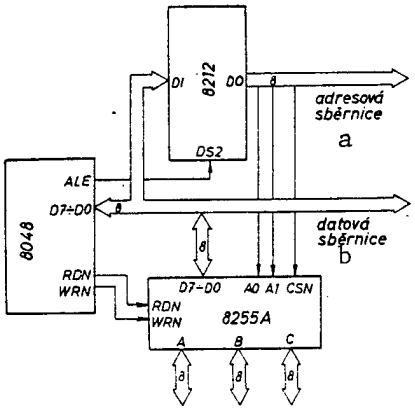

Fig. 11. Expansion of Number of I/O Lines With Channel 0

Key:

a. Address bus

b. Data bus

The circuit designated as the 8243 expander contains four 4-bit bidirectional static channels with input buffers (P7-P4). Data transmission between the microcomputer and the expander is achieved by connecting 4-bit channel P2 to pins P23-P20. Data transmission is unambiguously controlled by the signal STBN. Operating the expander requires that a low input be fed to the CSN select input.

The 8243 is produced by the same technology as the 8048. It is packaged in a 24-pin DIL package with the pin assignments shown in Fig. 12. The 8243 is connected to the 8048 microcomputer as shown in Fig. 13. Automatic initialization of the expander after connection of the power supply voltage U_{CC} is provided in hardware: Channel pins P7-P4 are set in the third state (input mode) and channel P2 waits for data from the microcomputer. The expander is initialized whenever voltage U_{CC} falls below 1 V regardless of the condition of signal STBN.

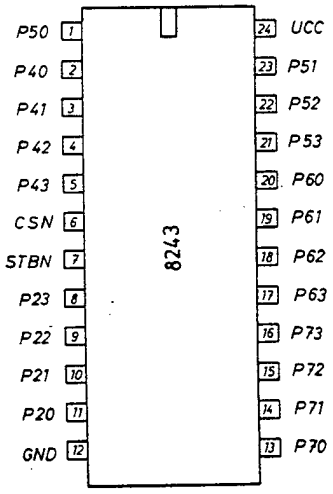

Fig. 12. Pin Assignment of 8243 Expander

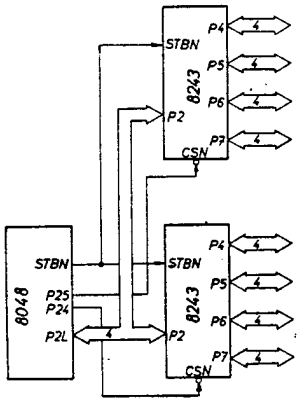

Fig. 13. Connection of 8243 Expander With 8048 Microcomputer

The circuit design of the expander is relatively simple, and we will confine ourselves to the parts of the circuitry which, as shown in Fig. 14, directly determine the functional characteristics of channels P7-P4. The control signals in Fig. 15 are derived from the signal STBN which synchronizes communications between the 8048 and the 8243.

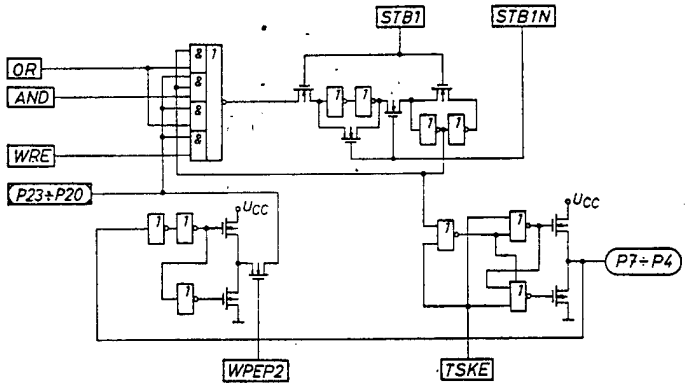

Fig. 14. Connection of Channel P7-P4 of 8243 Expander

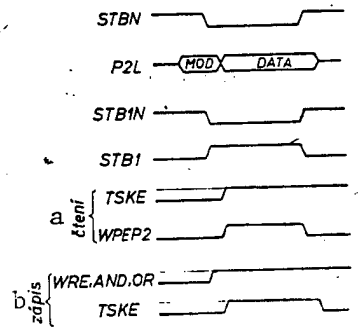

Fig. 15. Control Signals for Functions of 8243 Expander Channel

Key:
a. Read
b. Write

At the rear edge of signal STBN the 8048 microprocessor emits bits of information (MOD) which are generated automatically with reference to which instruction is controlling data transmission. The contents of MOD select one of four channels P7-P4, and this channel is set in one of four functional modes. The allocation is described by Table 7. Actual data transmission to expander 8243 is concluded on the rising edge of STBN, which thus indicates the end of data when reading into the microprocessor.

Table 7. Coding of Contents of MOD for Control of 8243 Expander

P23	P22	[a] Režim	P21	P20	[b] Kanál
0	0	[c] čtení	0	0	P4
0	1	[d] zápis	0	1	P5
1	0	OR	1	0	P6
1	1	AND	1	1	P7

Key:

a. Mode
b. Channel
c. Read
d. Write

As shown in Table 6, the transmission of data between the microcomputer and expander is controlled by four instructions (MOVD A, Ppe controls reading of data into the microcomputer; MOVD Ppe, A controls entry of the lower half of the accumulator (ACCL) into the output buffer of the expander channel; and ANLD Ppe, A and ORLD Ppe, A set the contents of the expander output buffer in accordance with the results of a logical operation involving the buffer ACCL and the initial content of the channel buffer). The activity associated with transmission of MOD is the same for all of these instructions. It can be seen from Table 3 that the information is in the output buffer of channel 2 (OBD2L), and thus at pins P23-P20, before the rear edge of signal STBN arrives. In the case of instructions MOVD A, Ppe, the output of the selected channel is put in the third state by signal TSKE and signal WPEP2 is activated, transmitting to pins P23-P20 the data fed to the pins of the decoded channel. Transmission of data on the internal bus of the microcomputer requires that during the read operation the output buffer OBD2L be high. We saw the reason for this requirement earlier in the description of the operation of channel 2. This instruction activates signal G1P2L, which, as shown in Fig. 7, sets buffer OBD2L high. The actuating signal WP2DB, which results in writing onto bus DB, is generated at period T3, i.e., immediately after the rising edge of signal STBN. Since data are defined only at pins P23-P20, but the states of all pins of channel 2 are transferred to the internal bus, the control unit clears the upper half of internal bus DB during the transmission of data to accumulator ACC. After completion of the read operation the channel remains in the third state but the transmission channel is disabled because WPEP2 is low.

The other three instructions transfer the contents of the lower half of the accumulator (ACCL) into output buffer OBD2L and thus to pins P23-P20. If the contents of MOD have set the read mode, the signal WRE is activated, allowing the contents of the output buffer of the selected channel to be set in accordance with the contents of ACCL. The third state of the output is terminated at the same time (TSKE low) and the channel pins are set in accordance with the contents of the output buffer. This state is latched and the state of the output is changed only when new data are written into the same output buffer of the expander channel.

If the contents of MOD have activated either an AND or an OR signal, the data written in the output buffer of the selected channel depends on the

value in accumulator ACCL and the initial content of the output buffer. The operations are rather easy to understand and can be followed from Figs. 14 and 15.

The output amplifiers of channels P7-P4 have a considerably higher current capacity than the outputs of the microcomputer themselves (sinking of one TTL gate). The power capacity of the expander is indicated by the fact that each of 16 pins can carry 4.5 mA (max total of 72 mA). A single pin can handle a current of up to 10 mA.

In practice, the individual expander channels are most often used for one-directional data transmission. If we want to change the mode of operation of the expander channel from the output to the input function during processing of a user program, it is recommended that the result of the first read operation be ignored. This rules out the possibility that the output data might be affected by the state of the input amplifier, which is not yet in the third state.

3. Another possibility for expanding the number of microprocessor lines is associated with pins TEST0, TEST1 and INTN. The data fed to them may be specified by the output of some switch (multiplexor, interrupt system and the like). The addresses of the input to which it is connected may be designated, for example, by the pins of channel 1. This principle is illustrated in Fig. 16.

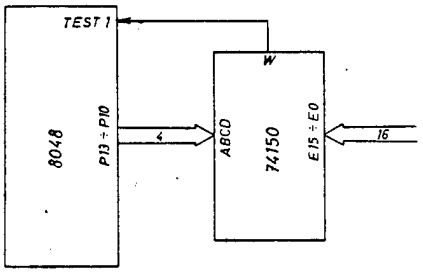

Fig. 16. Expanding Number of Output Lines of 8048 by Means of 74150 Multiplexor

Program Interrupt

Program execution by the 8048 may be interrupted in three ways:

a. by the signal RESETN = L,

b. by reception of an external interrupt request generated by setting the input INTN low,

c. by reception of an interrupt request as a result of overflow of the internal counter CT.

Program interrupt by the signal RESETN = L is nonmaskable. The microprocessor is reset by the following operations:

--clearing the program counter PC;

--clearing the stack pointer SP;

--setting flip-flop BS low, which makes registers R0-R7 (register bank 0) directly addressable;

--setting flip-flop DBF high, which selects program memory bank 0 (PC + 000H-7FFH);

--setting channel 0 pins in third state (static input mode);

--setting a logical 1 in the input buffers of channels 1 and 2, enabling input of data to the microcomputer through these channels;

--blocking of the reception of external interrupt requests or counter requests (CT);

--cessation of counting by counter CT or cessation of change of its contents;

--clearing of flag TF, which indicates overflow of CT;

--clearing of software flags F0 and F1;

--cessation of output of phase FV on pin TEST0 if this mode has previously been activated by the instruction ENT0 CLK.

The signal RESETN must be low for a certain minimum amount of time. If the signal is externally generated it must last for at least 50 ms from the moment when the voltage U_{CC} reaches the minimum working level. In most practical cases the 8048 is initialized by the circuit shown in Fig. 17. Pushbutton T and resistance R produce the required initial state of capacitor C, i.e., discharge. When pushbutton T is disconnected or the microcomputer is connected to power source U_{CC}, the capacitor, with a recommended capacitance of 1 microfarad, begins to discharge through resistance R_{in}, which is part a component of the microcomputer. The rising voltage on capacitor C is handled by a Schmitt trigger, which is part of the microcomputer's control unit. The trigger output automatically assures that the L level, on the basis of which the control unit sets the conditions for initializing the 8048, lasts for the required amount of time.

The RESETN pin is also used for reading the contents of internal memory, which will be described in detail later.

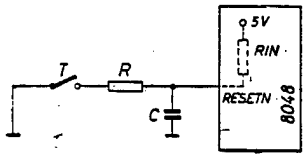

Fig. 17. Connection of RESETN Input of 8048 for Automatic Reset

Processing of external or counter interrupt requests differs fundamentally from the activity initiated by signal RESETN = L. In the first place, both of these interrupts are maskable and the processing is similar to execution of the CALL instruction. The only difference is that the instruction opcode and second byte are generated directly by the control unit. Therefore, external interrupts and counter interrupts result in storage of the contents of the program counter PC and the status word PSWH in the stack at the address designated by the stack pointer SP. The entire subroutine which processes the interrupt (including all possible subroutines) may be located in bank 1 of program memory, because the content of bit PC11 is fixed at zero for the entire period of interrupt processing and cannot be changed by execution of instructions SEL MB1 and CALL or JMP.

The interrupt servicing subroutine is ended by the execution of instruction RETR. This means that if the interrupt request processing subroutine contains a call of one or more additional subroutines, the return from such subroutines must be made by the instruction RET.

It is recommended that only one interrupt level be used in the 8048. If an interrupt request is received, the hardware prevents reception of any other request until the instruction RETR is processed. There is theoretically a way of circumventing this limitation: this involves calling a dummy subroutine and returning from it by instruction RETR. In this way the interrupt servicing subroutine is not concluded but it is possible to accept further interrupt requests.

The counter CT may operate as a counter or timer. An interrupt request is produced every time the counter is filled if a counter interrupt is enabled. This makes it possible to produce another type of external interrupt by setting the counter CT, operating as an event counter, to the value OFFH, so that the first event at pin TEST1 results at in an interrupt.

If counter CT is used as a timer and processing of an external interrupt request lasts longer than the time between two requests from the counter, one of the interrupt requests will be lost and a fault will result. This can be handled by introducing instruction JTF into the programs and subroutines often enough so that the time interval between JTF instructions will not be longer than the time period generated by counter CT.

We will now describe the processing of an interrupt request in the course of a program by the 8048, with the help of Fig. 18. Flip-flops PPCT (counter interrupt enable) and PEP (external interrupt enable) are directly controlled by instructions (EN TCNTI and DIS TCNTI, EN I, DIS I) or by the

signal RESETN. Thus it is apparent that either or both interrupts can be enabled.

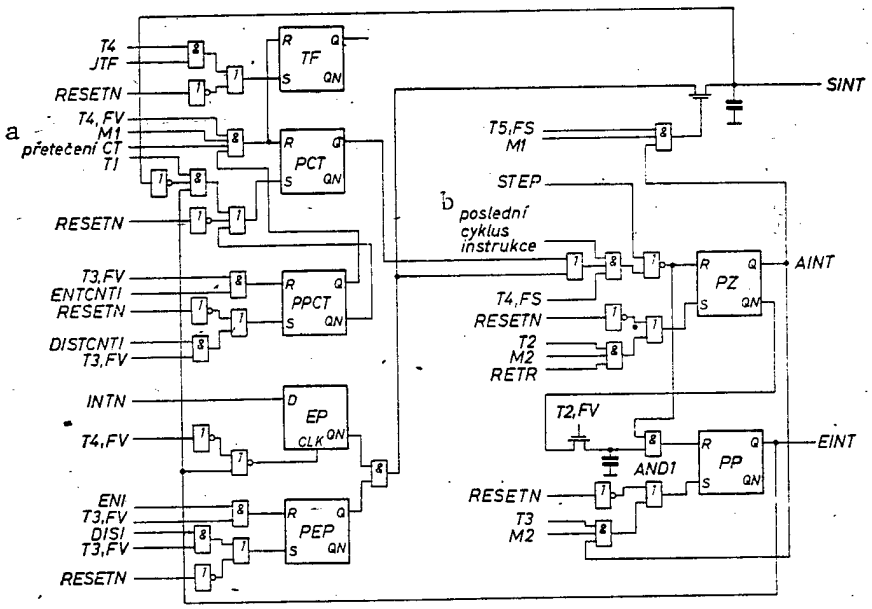

Fig. 18. Wiring of Logic Circuit for Processing of Interrupt Request in 8048

Key:

a. Overflow

b. Last instruction cycle

Flag EP (external interrupt) carries information as to whether or not there is an external interrupt request, and flag PCT is set if an interrupt from counter CT is enabled and the counter has overflowed. In addition, each overflow of counter CT sets flag TF (Timer Flag), which can be cleared only by execution of instruction JTF or by the signal RESETN = L.

Before we proceed with the description, we must note that every RS flip-flop is cleared by the signal RESETN during initialization. It must also be borne in mind that a controlled switch with parasitic capacitance at the output behaves like a D flip-flop. Thus, for example, in every period T2, FV, the negatived output of flip-flop PZ is sampled, which means that every input at gate AND1 is high.

If an interrupt request is made and enabled, then during period T4, FS of the next instruction flip-flop PZ and flip-flop PP are set and the signal AINT = H causes the following functions:

--holds PC11 low during processing of the interrupt,

--produces clearing of flip-flop PP and sampling of signal SINT.

Similarly, signal EINT = H produces the following functions:

--blocks generation of signal WROMDB which transfers the content of ROM memory to the internal bus DB,

--produces clearing of flag PCT,

--generates CALL instruction (opcode 14H) on internal bus via the control unit in period T1 of the first machine cycle,

--blocks incrementation of program counter PC during execution of forced CALL instruction.

The CALL instruction is written into the instruction register IR and its execution results in storage of the contents of program counter PC and part of the status word PSWH in the stack at the location addressed by stack pointer SP.

The signal SINT which is sampled during period T5, FS in the first machine cycle M1 carries information on the type of interrupt (high = external interrupt, low = counter interrupt). Signals SINT and EINT together force the address of the interrupt that has been received onto the internal bus during period T1 of the second machine cycle (for an external interrupt it is address 003H, for a counter interrupt address 007H). This address is written into program counter PC and execution of the interrupt processing routine begins from this address. If requests for both interrupts arrive simultaneously, signal SINT is set high and the external interrupt is processed first. But the request for a counter interrupt is not lost: it is stored in flag PCT and processed immediately after the end of the external interrupt.

During processing of the forced CALL instruction, flag PCT is cleared if a counter interrupt has been received (SINT low and EINT high). In addition, flag PP is cleared, but flag PZ remains set until the instruction RETR is executed. This prevents reception of another interrupt, for the complemented output of flag PZ feeds a logical 1 to gate AND1 and thus flag PP cannot be set.

In interrupt processing, good use can be made of the existence of two groups of directly addressable registers in internal data memory. When calling the interrupt servicing subroutine, the register bank is switched, e.g., from 0 to 1, by the instruction SEL RB1. This means that the data in bank 0 is saved and the instruction operates with register bank 1. On return from the subroutine, switching from bank 1 to bank 0 is achieved by execution of instruction RETR, which also restores the content of flag BS.

Transfer of one bit of information from the subroutine to the main program can be effected by means of flag F1, which is not affected by execution of the instruction RETR.

Reading of Program From External Program Memory (External Access)

The 8048 operates in this mode if one of the following conditions is met:

1. If the output to EA receives a logical 1 (5 V), the entire program memory is located outside the microprocessor. The input RESETN must be low when a high level is fed to EA.

2. Input EA is low but the content of program counter PC has been incremented above the internal program memory capacity, i.e., (PC) > 3FFH.

The way in which the 8048 reads the program from external ROM memory is briefly described as follows:

--The microcomputer transmits the address from the program counter and transfers the contents of PCL to the output buffer OBD0 and the contents of counter PCH to the pins of channel 2L (P23-P20). The contents of PCL are transferred to buffer OBD0 via the internal bus during period T2 of the first machine cycle or period T3 of the second machine cycle. In these periods, the internal bus holds the content of PCL which addresses the next instruction, and this is written in output buffer OBD0 by the signal GDBD = H. In addition, instructions involving channel 0 are prevented from using it during transmission of the contents of PCL. Here it must be realized that the instruction OUTL BUS, A is executed, but loses its static character. This means that the current data sent out by instruction OUTL BUS, A is at the pins of channel 0 (D7-D0) only when the WRN signal is active. Program counter PCH is directly connected to the pins of channel 2L. The transmission is not made through output buffer OBD2L and thus does not affect its content. Since the current address is at pins P23-P20 from period T3 on, the static character of the output of the lower half of channel 2 (instruction OUTL Pp, A) is again disabled. Otherwise its function is not affected.

--The signal ALE = H writes the address in the external program memory buffer. In most practical applications it suffices to write only the contents of counter PCL in external memory, thus freeing up the output buffer of channel 0.

--The signal PSENN = L releases the data from ROM external memory onto the system bus (D7-D0). In period T1 of M1 or T1 of M2 (two bytes) the instruction reaches the external bus via channel 0. This occurs at the same time as in reading from internal ROM memory, so that there is no difference in the subsequent processing of the instruction. Signal PSENN is automatically generated in reading of the program from the external memory. The generation and form of signal PSENN depend on the type of instruction: the three possible shapes are shown in Fig. 19.

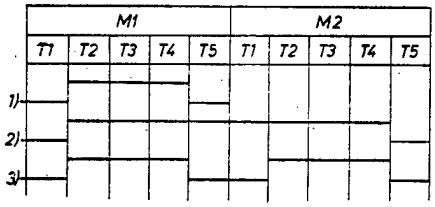

Fig. 19. Waveforms of PSENN Signal for Different Types of Instruction: 1--One-byte, one-cycle; 2--One-byte, two-cycle; 3--Two-byte, two-cycle

Single Step Mode

This mode makes it possible to trace the processing of the program by stepping through it instruction by instruction. Activation of this mode requires that a low level be fed to input SSN (Single Step Not). In this mode, the entire instruction is always executed. The requirement of completion of the instruction is assured by having the input SSN sampled only in period T3, FV of the next cycle of execution of the instruction. At this moment, as shown in Fig. 20, a step signal is generated, putting the 8048 in the STOP state. Single stepping requires that the SSN signal go low before time T3, FV of the last machine cycle of the preceding instruction. The STOP state of the 8048 microcomputer involves the following activity:

--In period T1, the control unit writes the code for the NOP instruction on the internal bus, and it is loaded into instruction register IR. During execution of the NOP instruction, the STEP signal prevents incrementation of the program counter PC, which preserves the correct address of the next instruction.

--During period T2, the contents of counter PCL are loaded into output buffer OBD0. Clearly, the instruction OUTL BUS, A loses its static character.

--During period T3, the contents of counter PCH are fed to the pins of channel 2L, while the contents of the channel 2 output buffers (OBD2L, OBD2H) are not changed.

--Signal ALE goes high.

--The 32X divider is stopped.

--Signal PSENN is blocked.

--Acceptance of interrupt requests is disabled.

The STOP state ends whenever the signal STEP goes high or when a high level is found at the SSN input.

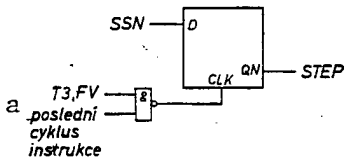

Fig. 20. Activation of Single-Step Mode in 8048

Key: a. Last instruction cycle

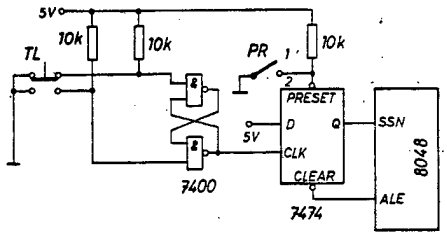

Fig. 21. Connection of External Circuits for Single-Step Mode

An example of the connection of external circuits for single stepping is shown in Fig. 21. The switch PR enables (position 1) or disables (position 2) single stepping. The actual stepping is done by means of push-button TL.

The ROM Internal Program Memory Read Mode

The ROM internal program memory read mode is used for checking the correctness of the user program loaded into it. If it is set, 12 V is fed to input EA. When the 12 V is applied to EA, the RESETN input must be low. The 12 V potential at EA activates the 8048 for the following actions:

--It forces the opcode of the NOP instruction onto the internal bus at T1, M1 and uses special logic to assure its execution in two cycles.

--It blocks signals WPCLDB, WALUDB and WMDB, which allow writing on the internal bus.

--It blocks the effect of the signal RESETN = L, which under other conditions could activate at input EA the activity associated with initialization of the computer (see description of interrupt processing).

--It prevents production of the EXROM signal, which is activated if the 8048 is in a system with external ROM program memory.

The level of signal RESETN is sampled in every period T4. An external RIROM signal is produced (Fig. 22) whose value shows the direction of transmission. If RIROM is low, the information is transmitted from the input of channel 0 and the lower half of channel 2 to program counter PC in the following manner:

--At time T2, M1 the address is transmitted from the input of channel 0 to register PCL;

--At time T2, M2 the address is transferred from the input of channel 2L (P23-P20) to register PCH.

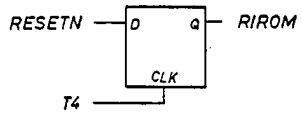

Fig. 22. Control of Operation of 8048 When Reading Contents of ROM Internal Memory

This activity is repeated as long as the RIROM signal does not change. When RIROM is high, the content of the addressed location is transmitted during period T1, M2 to the output buffer of channel 0 (OBD0). In addition the third state of pins D7-D0, which had been set in accordance with the contents of OBD0, is disabled.

To prevent faults in this mode, it must be assured that the signal RESETN is at the requisite level for at least two machine cycles. Fig. 23 shows one possible circuit for reading the contents of ROM internal program memory in the 8048.

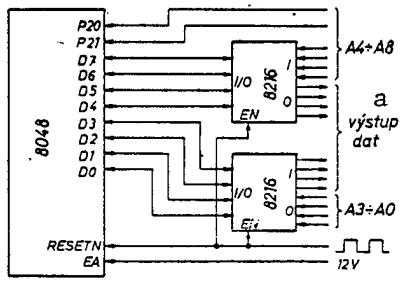

Fig. 23. Circuitry for ROM Internal Memory Read Mode

Key: a. Data output

Standby Power Mode

The 8048 may be put into the standby power mode, which has only 10-15 percent of the normal power requirement. In it, operation of the microcomputer ceases, but the data in internal RWM data memory is saved. The standby power mode is used particularly in power outages, when the microcomputer is switched to backup battery power supply.

The 8048 has three power supply circuits (Fig. 1):

U_{DD} = 5 V: the power supply of the RWM memory and internal substrate bias generator;

U_{CC} = 5 V: the power supply for the rest of the chip;

GND = 0 V: electrical ground.

In the standby power mode, power is fed only to input U_{DD}, while U_{CC} may be disconnected. The voltage U_{DD} powers not only RWM data memory, but the substrate bias generator U_{BB}, which assures correct operation of the transistors in this circuit.

The actual activity in the transition to the standby power mode during a power outage is shown in Fig. 24. External circuits are used to monitor the power supply level. If it falls below a specific boundary value U_H the external circuits generate a signal requesting an interrupt. The computer reacts to this interrupt by executing a routine that includes the following operations:

--It stores the required information (contents of accumulator ACC, program counter PC, status word PSW and possibly of counter CT and the output buffers of channels 0 and 2) in RWM internal data memory.

--It switches the U_{DD} power input to the backup supply.

--It sets the input RESETN low (capacitor C in Fig. 17 discharges).

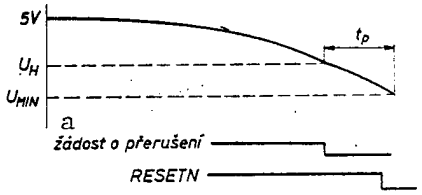

Fig. 24. Handling of Voltage Drop and Changeover to Standby Power Mode

Key: a. Interrupt request

This assures that the data in RWM data memory are unchanged. But it is necessary to assure that time t_p in Fig. 24 is always longer than the time required for execution of the subroutine used to deal with the drop in the power supply.

Return from the standby power mode is achieved by again connecting the voltage to input U_{CC}. As shown in Fig. 17, application of voltage to input RESETN produces the required initialization of the 8048.

The Oscillator

The chip containing the 8048 also holds an oscillator for frequencies of 1-6 MHz which can operate in three possible modes:

1. A crystal with a frequency of 1-6 MHz connected between inputs XTAL1 and XTAL2 as shown in Fig. 25.

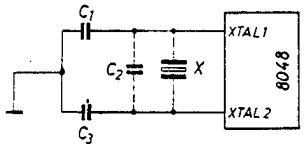

Fig. 25. Control of Internal Oscillator by Crystal

2. If the frequency stabilization requirements are not stringent, an LC circuit may be used as shown in Fig. 26. The magnitude of the induction L and capacitance C_1 and C_2 depends on the frequency. For example, when the inductance is L = 120 microhenries and the capacitances are $C_1 = C_2 = 20$ picofarads, the oscillator will operate at a frequency of about 3.2 MHz.

3. The frequency is imposed from an external circuit as shown in Fig. 27. Since inputs XTAL1 and XTAL2 are not compatible with TTL logic, resistances R1 and R2 are provided to increase the H logical level.

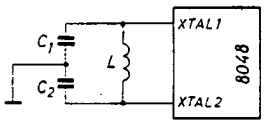

Fig. 26. Control of Internal Oscillator by LC Circuit

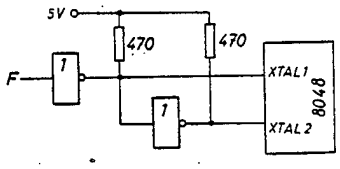

Fig. 27. Control of Internal Oscillator From External Source

Conclusions

We have acquainted ourselves with the operating principles and characteristics of the 8048 single-chip microcomputer, which is a typical representative of the 48 series. Integrated circuits with properties equivalent to those of the 8048 and 8038 types and, somewhat later, of the 8078, will become available to Czechoslovak users during 1984. In addition, the assortment of associated integrated circuits will be increased to include the 8243 expander, the 2716 EPROM memory, and the 6561 RWM memory, produced in CMOS technology with 256 x 4 bit organization. Adding to this the availability of various types of associated circuits as a result of domestic production or import from the Soviet Union for microcomputers using the 8080A microprocessor, or as a spinoff from the production of 4000 series CMOS circuits, most potential purchasers will have to admit that there is a reasonable selection.

Unfortunately, expansion of the scope of integrated circuits used or provided does not solve the problem of incorporating electronics into our industry. The availability of circuits is a necessary but not sufficient condition. Without changes in management and the creation of effective pressures, the large-scale introduction of electronics into our industry will not be achieved, and many attractive plans will remain merely fond hopes.

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ACHIEVEMENTS AND PROBLEMS OF DOMESTIC TELECOMMUNICATIONS RESEARCH AND DEVELOPMENT

Budapest HIRADASTECHNIKA in Hungarian No 8-9, 1983 pp 342-347

/Article by Dr Gyula Tofalvi, Telecommunications Research Institute Commissioner for the OKKFT A/5 and OTTKT K/8 programs: "Achievements and Problems of Domestic Telecommunications Research and Development"/

/Text/ Dr Gyula Tofalvi studied at the Budapest Economic Sciences University and then at the Budapest Technical University. He obtained a degree in electrical engineering in 1954. Between 1954 and 1975 he worked at the Electromechanical Enterprise where he was a researcher, developer, laboratory chief, chief of the development main department and chief engineer of the enterprise. During this period he worked on medium, short and ultrashort wave transmitters and antenna systems on black and white and color TV transmitters and on stero quadrophone transmitters. Between 1975 and 1980 he was technical vice president of the Hungarian Signal Technology Association. In this period he dealt with the development of the Hungarian electronics industry with special emphasis on the development of the signal technology industry and parts industry. Since 1980 he has been scientific director of the Telecommunications Research Institute. He was awarded the Kossuth Prize in 1959. In 1979 he became a director of technical sciences. In 1981 he received the title of university professor.

Summary

The article gives a comprehensive picture of the research and development efforts, achievements and problems of Hungarian telecommunications. It discusses research and development goals in a system of boundary conditions for world telecommunications development. Special emphasis in the comprehensive article is given to the cooperation which developed in the wake of the OKKFT /National Medium Range Research and Development Plan/ A/5 and OTTKT /National Long Range Scientific Research Plan/ K/8 programs, cooperation which developed among enterprise, institutional, college, university and Postal research sites. The author unveils with shocking frankness the serious situation deriving from the backwardness of the Hungarian electronics background industry and the consequenes which can be expected. At the same time he presents with the preciseness of an expert possible ways out in the given situation. His final conclusions are as much a criticism of the

industrial development of the past decade as they are a conception for the possibilities for a solution in the years ahead.

Introduction

People want to talk with one another!

Even people who live far from one another want to talk with one another.

Even those who still cannot be "contacted" today want to talk with one another.

Even modern machines want to"talk" with one another.

Even the processes and phases of processes want to "talk" with one another.

People and even machines "want to talk with one another." The need for conversation on a world scale has arisen, and this can be satisfied only by a modern telecommunications world network. And even this is not the end! The information needs of people are constantly increasing.

The social, technical and economic development of the world requires a development, more dynamic than ever before, of the recording, storage, transmission, management, processing, etc. of information. If we are to be able to satisfy the communication needs of people, machines and processes we will need ever newer, information transmission channels, which can be provided only by putting into service ever newer transmission procedures, equipment, systems and networks.

Expanding telecommunications services--bringing in new sources of information and processors of information--will require not only a swift increase in the number of transmission channels but also an improvement in the use efficiency of already existing transmission channels. Figures 1, 2 and 3 illustrate models of networks satisfying the communication needs of people, machines and processes and the information needs of people. A qualitative development of telecommunications networks will require the realization of new transmission procedures, new transmission paths, new transmission media, new frequency domains, greater signal transmission speeds than ever before, greater transmission band widths than ever before, etc. Telecommunications research and development around the world are in the service of these aspirations.

Research and Development Goals

Realizing a qualitative and quantitative development of telecommunications networks thus poses a number of new tasks for research and development. To mention just a few of these, a further development of digital signal transmission is in first place in research and development on new transmission procedures. In addition:

--working out new solutions is possible in the wake of the convergence of telecommunications and computer technology;

--a further development procedures connected with speech analysis and synthesis;

--cheap, highly reliable satisfaction of mass needs;

--perfecting extended spectrum signal transmission procedures;

--working out the new solutions to be expected in the wake of the convergence of broadcasting and telecommunications;

--realizing dynamic channel assignment depending on traffic;

--introducing new solutions which will help remote data processing become a mass service;

--developing and using procedures which will aid telecommunications network integration and the integration of telecommunications services.

In the area of new transmission paths research and development on procedures and equipment connected with a further development of information transmission via artificial satellites is significant while in surface transmission we have primarily work on the development of networks helping to bring in new areas, new information sources and processors. In the area of new frequency domains research and development on bringing in millimeter wave lengths, 15-100 GHz, seems necessary, naturally together with the 0.8-1.6 micrometer wave length domain to be brought in by light telecommunications. In the area of increasing signal transmission speeds research and development connected with signal speeds of several hundred Mb per second and then Gb per second represent a closed program. Most significant among new transmission media is the use of light conductive fibers, which promises to be a research and development program of decades.

According to a number of opinions atmospheric light telecommunications will play a special role in information transmission also.

With the aid of light conducting fibers one can create channels of such large capacity that they can be used at most only in part by services which can be imagined today.

Surface telecommunications will achieve unimaginable channel capacities with the use of light conducting fibers. By which is to be understood not only long distance, high capacity signal transmission but also mass use of small distance, small capacity transmission sections, and even the building of telecommunications networks to the subscribers.

The use of light conducting fibers will have a determining role in the realization of the integration of telecommunications services and of the convergence of broadcasting and telecommunications. Realizing integrated digital

telecommunications from subscriber to subscriber can be solved optimally only by making light transmission an everyday practice.

Another large area for research and development is increasing the utilization of existing channel capacities and those to be built--for example, forwarding message packets, computer organization of channel access, developing intermediate storage, putting new sequencing procedures into operation, etc.

After this brief review of the developmental trends in the electronics world let us give a few thoughts about the chief themes, aspirations, achievements and problems of domestic research and development.

Achievements of Domestic Research and Development

Two large programs for the years 1981-1985 sum up the research and development work for domestic telecommunications technology:

--the OKKFT A/5 medium-range research and development themes; and

--the OTTKT K/8 long-range research and development themes.

The OKKFT A/5 program divides the conduct of research and development work among three sub-programs:

--sub-program A embraces systems technique questions;

--sub-program B embraces switching techniques; and

--sub-program C embraces landline and wireless transmission technology tasks (figure 4).

The responsible leader of the program is the appropriate deputy minister of the Ministry of Industry, whose work is aided by the Program Council and the Program Commissioner. Operational guidance of the several sub-programs is provided by the TKI /Telecommunications Research Institute/, the BHG /Beloiannisz Telecommunications Factory/ and the TRT /Telephone Factory/ and TKI respectively. The research and development tasks of the long-range themes belonging to the OTTKT K/8 program were grouped around six Main Themes (figure 5). Even this order for research and development illustrates strikingly the coordinated joint work on which the solution of the tasks of the program is based. Figure 6 shows even more strikingly the broad, comprehensive cooperation. In it one can see that the program is being realized in the creative cooperation of telecommunications enterprises, telecommunications researchers, university and college researchers, the most potential Hungarian users and the appropriate high level authorities.

Special mention must be made in this cooperation of that everyday, common work, long awaited and realized in these two programs, which has been established finally between the research sites of universities, colleges and the Hungarian Post Office, on the one hand, and industrial researchers and industrial producing enterprises on the other.

I know that a number of enterprises worked well with the several university faculties and the several institutions of the Hungarian Post Office in the past also, but what has been established in this program represents more in content. The cooperation of an entire branch of industry has been realized in this program, not only with the several faculties of university (or college) or with the several areas of the Hungarian Post Office, but comprehensively, extending to every area and theme which the development of telecommunications defines for us. It is thanks to this creative cooperation that this cooperation is concentrated not only on the joint solution of individual research and development, themes, but rather on long-range tasks also, and beyond these on such significant questions as a quantitative and qualitative further development of university teaching and research bases, the further training of experts working in industry, aiding the publication of professional telecommunications books in Hungarian and foreign languages, joint discussion of teaching and research programs, etc. Thanks to the cooperation of university and industry a coordinated representation has been realized in the professional committees of the Academy also. It is well known that we have achieved a number of nice results in the course of work done within the framework of these two programs in the two and a half years which have elapsed thusfar, but let me list among the most beautiful and most significant of our achievements that cooperation which was realized in these two programs!

Let me mention a few of our significant achievements of the two and a half years which have elapsed:

--in the area of research and development on systems the results achieved thus far in research and development on a subscriber radio telecommunications system and the PGM rural or suburb system;

--in the area of switching techniques the work done thus far in adopting the stored program controlled, time sharing culture, in research and development on this and in developing equipment using this principle. Of crucial significance not only for the BHG but also from the viewpoint of the entire Hungarian telecommunications industry are the results achieved thus far in preparing to adopt licenses belonging to this culture;

--in the area of landline transmission technology the development of the several levels of the PGM hierarchy and starting research and development on light communications in the area of both landline and atmospheric transmission;

--in the area of wireless transmission technology the procedures, equipment and systems realized thus far in increasing frequency ranges, in digital signal transmission and in developing tunable systems;

--system plans, circuits, equipment, etc. worked out in research and development on on-board and earth equipment connected with satellite communications.

I could talk long and with pleasure about the results achieved thus far in our telecommunications research and development, but I think that even this

great celebration today does not justify our celebrating at half-time. The ever more difficult environmental conditions caution us to think modest and reserved behavior also.

Problems of Our Research and Development

If someone had asked me years ago, for example at the time of working out the medium-range and long-range research and development programs described in outline above, what the biggest problems of our telecommunications research and development were, I would certainly have mentioned:

--a development of electronics swifter than ever before;

--the realization of research and development with a system view;

--a race with market or fashion obsolesence times which are ever shorter;

--a concentration of our research and development resources and assets based on cooperation;

--standardization;

--supplying research and development with suitable tools, etc.

Today, as we celebrate the World Year of Telecommunications, there can be no doubt that the biggest problem of our telecommunications research and development is the unfortunate situation which has developed in the supply of industrial primary materials and parts and the further problems which can be expected from this.

The source of the problem can be found in the fact that, together with the backwardness of our primary materials and parts industry, the difficulties arising with capitalist import have made questionable the further success of our medium-range and long-range research and development programs, have even made questionable the perfect realization of the programs which have given valuable results thus far. Access to the most modern tools is a vital condition for research and development, and research and development based on obsolete primary materials and parts would mean wasting our intellectual resources. Beyond the immediate effects of the problems deriving from the supply of primary materials and parts it can be expected that the second, third and further order indirect effects of the enterprise solutions possible in the given situation will create enhanced difficulties for our research and development. Not every alternative of the enterprise self-protection policies necessarily developing in the given situation can be made compatible with the capabilities and conditions of our telecommunications research and development bases.

Let us list the components of our present situation and examine in parallel with this the problems of our research and development.

The result of the examination of conscience made by our electronics industry at the beginning of the Sixth Five Year Plan can be summed up in the follow points: 1. Decades of growth of our electronics industry were characterized by an uneven qualitative and quantitative development in which there grew up, behind a dynamically growing equipment and apparatus manufacturing industry, a background industry which was backward both qualitatively and quantitatively. This backwardness developed not only in comparison to the world electronics industry but also in regard to the domestic needs, including the needs of our equipment manufacturing industry therein. The decades of struggle for a comprehensive development of the parts industry brought only partial results and instead of a proportional development of the background industry we chose the most dangerous emergency solution, replacing it with capitalist import. 2. Even making use of world primary materials and parts, on the free competition capitalist market, our equipment manufacturing industry could produce only products which were by and large, difficult to sell or could not be sold at all. The virtually endless ability of the socialist market to receive goods fed the extensive development of the equipment manufacturing industry in the 1970's, naturally with a background industry supply at a time when industry was ensured the unlimited satisfaction of an exponentially increasing capitalist primary materials and parts demand. A significant proportion of our capitalist export successes could be broadened only on protected or oriented markets.

It is well known that a significant role was played in such a development of our electronics industry by industrial, economic and international factors, in addition to enterprise factors.

Thus, to a crucial extent, the supply of primary materials and parts for our electronic equipment manufacture was based on capitalist import, with which there was no special problem as long as the economy could provide the dollar cover for it without further ado. A radical change came in 1982 when producing the dollar cover necessary to ensure capitalist import became increasingly more difficult and in the present situation we have reached the point where a number our enterprises have put on the agenda an analysis of ways out. We must see that the consequences of an industrial policy emphasized for decades and which promised a future, and at the same time the consequences of an industrial practice which was faulty and erroneous, cannot be bridged over now without sacrifices. We must see also that there are many among us who believe that if we do not talk about our problems then they do not exist and if we turn away from the problems then we are not responsible for them.

The only path I recognize as promising a solution, under socialist social relationships, is for the dialogue between the leaders and led to be more open, more frank and more democratic the more serious the problems to be solved. I mention this awareness of responsibility in connection with the problems of our research and development also. We must face the fact that for the time being the background industry solution created by unlimited dollar cover has come to an end in the life of the Hungarian electronic equipment and apparatus manufacturing industry and the mistakes we made during the great extensive development of the 1970's cannot be escaped from with impunity.

Amidst the present troubles new life must be given to:

--the warnings voiced, in the interest of a stressed development of the Hungarian electronic parts industry, at the parts conferences of the Signal Technology Scientific Association in Pecs, 1974, Szeged, 1975, Szekesfehervar, 1977, Kecskemet, 1978, and Szombathely, 1979;

--the expert analyses and syntheses in a series of industrial conceptions prepared over the decades and realized only in part or never realized, which called attention to the consequences and dangers of a disproportionate industrial development.

The problem which has arisen can be cause of satisfaction for no one, especially not for those who now see themselves surrounded by problems of the size they predicted. Whatever happened in the past decade, we can have only one obligation now, to seek ways out and come to solutions.

What ways out can there be for us when, together with our primary materials and parts background industry backwardness, our difficulties with capitalist import have increased also?

Boundary Conditions

1. Within the foreseeable future the domestic electronic primary materials and parts industry will not be in a situation where it can play a full, supply, background industry role for an electronic equipment and apparatus manufacturing industry of the size which has developed in our homeland at the beginning of the 1980's. Even today we can hope for more and more beautiful achievements in some parts categories (for example, microelectronics, hybrid circuits, etc.) but even with this we are far from having a primary materials and parts industry which can play the background industry role required either qualitatively or quantitatively.

2. Our access to socialist primary materials and parts cannot develop with the same speed as the difficulty with our capitalist import is increasing. The equipment and apparatus now being manufactured and planned for manufacture are the results of research and development of a time in which ensuring capitalist primary material and parts import did not yet present a problem. A sudden, impulsive switch from capitalist to socialist import would require the immediate solution of so many incidental tasks that they could be solved only in a completely new industrial behavior and at a gradual pace defined primarily by our intellectual resources. Switching from capitalist to socialist import is not a task of months, if it is to apply to electronic equipment manufacture as a whole, especially not after decades in which constraints of such a character did not appear in the everyday practice of industry. Beyond all this we must reckon with the fact that a switch from capitalist to socialist import would bring new problems as yet unknown (for example, in regard to instability, quality, price, etc.).

3. The appearance of our problems with capitalist primary materials and parts import involves substantive, formal and temporal warnings which re-

require from us not the solution of a temporary problem but rather the obligation to bridge over a longer range, profound period.

Ways Out Which Seem Possible for Our Electronic Equipment Manufacturing Industry

The domestic need for telecommunications equipment and apparatus--even including the consumer needs of society--is far smaller than would be able to provide a comprehensive program for an industrial branch of this size. Thus the realistic domestic market can provide a way out for only a small part of the capacity of our equipment manufacturing industry. Socialist export cannot be a way out for us at a time when the capitalist import needed for production represents such a large problem.

First Way Out

The most obvious way out, easiest to formulate but most difficult to realize, is a dynamic, indeed drastic, increase in the capitalist export of our equipment manufacturing industry--even taking into consideration the constraints of the given conditions. The successes and failures of our capitalist export in past decades, the world recession now raging, the result of our industrial examination of conscience at the end of 1980, our technical and technological level, our industrial practice developed in the course of past decades, etc. in themselves define for every understanding expert the reality of this. A gradual increase in capitalist export is a realistic goal for a number of enterprises, but this possibility is far from being a solution for our equipment manufacture as a whole, within a short time.

Second Way Out

Seeking capitalist manufacturing cooperation in which the primary materials and parts needed for production could be ensured through cooperation--even over the longer run. Let us say openly that we are talking about the possibility of capitalist jobwork. Even if we could count on this providing a partial or even complete solution for some enterprises, I do not believe that it could provide a solution for our equipment manufacturing industry at a time when extensive industrial development has come to an end in the world and only those can stay on their feet who can satisfy the requirements of intensive development, at a higher level than ever before. In this also the world recession presents merciless restrictions. We must seek this way out too, but we cannot expect from it a comprehensive solution of the problems of our equipment manufacturing industry.

Third Way Out

Seeking socialist manufacturing cooperation in which the primary materials and parts needed for production could be ensured through cooperation--even over the longer run. Let us say openly again that we are talking about the possibility of socialist jobwork. This also could bring results, but this alone could not provide a comprehensive solution for our equipment

manufacturing industry. It is well known that a number of our enterprises are talking about starting manufacture of Soviet research and development achievements which would solve the supply of primary materials and parts needed for manufacture of the given item.

Fourth Way Out

The gradual conversion of a part of the existing capacity of our electronic equipment manufacturing industry to the production of non-electronic products which could help in the increased creation of the balance of the national economy, by realizing capitalist export. Let us admit openly that this way out means a certain degree of retrograde development of our existing electronic equipment and apparatus manufacturing industry. It is not possible to judge today how deep this would go.

It cannot be my goal to come to a solution of the problems of a branch of industry within the framework of a celebratory presentation. My goal can only be, and this is my obligation as a program commissioner too--to evaluate the effect of the ways out which appear possible from the viewpoint of telecommunications research and development. One does not need too profound an analysis to establish that the four ways out considered can bring at most a partial solution for the manufacturing capacity of our equipment and apparatus manufacturing enterprises, perhaps rescuing them entirely in some areas.

But it must be added immediately that with the exception of the first way out every alternative posed is essentially opposed to research and development and realizing them would lead to the gradual decline of a part of our existing research and development base, created with the work and sacrifice of decades.

And, as usual, the problem brings new problems. With the growth of our primary material and parts import problems there appeared measures intended to limit the use of capitalist import primary materials and parts and there was no attention given--perhaps it was not possible--beyond the short range conception to factors which might make necessary a differentiation in the measures published. Manufacture and research and development were burdened uniformly with a 20 percent import fee, perhaps not considering, or facing and assuming the burden of the multiplying consequences. So that the effect of the measure should be complete in research and development also the import fee burdens the planned profit, which meant a reduction in developmental funds, wage development possibilities, etc. and awakened ideas in researchers and developers not every component of which can be regarded, in my opinion as progressive from the viewpoint of society and the economy (for example, mature, experienced, trained researchers are seeking new goals).

So far I have mentioned only one problem of our telecommunications research and development, but in my judgment the following problems remain significant also:

--getting the results of research and development into manufacture has become more difficult,

--MUFA /Technical Development Fund/ problems have appeared at several of our enterprises;

--research and development done at the expense of enterprise resources is proceeding more slowly than planned; etc.

To sum up, I feel that the implementation of the OKKFT A/5 and OTTKT K/8 telecommunications research and development programs formulated for the years 1981-1985 have brought, by half-time, results which are even more significant and better than planned. Concerning the second half I can say today only that even my thoughts are filled with unanswered questions.

And finally, let me confess that I have faith in the tension of the problems and ways out discussed. In what? I mean in the frankness with which we dare talk--among ourselves--aboutour problems and our search for solutions.

I thank the leadership of the HTE /Signal Technology Scientific Association/ for providing a forum for a discussion of our achievements and problems.

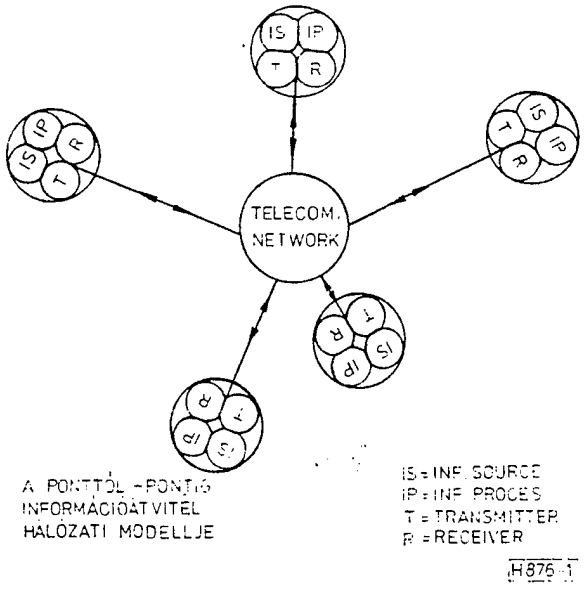

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Figure 1. Network Model of Point to Point Information Transmission

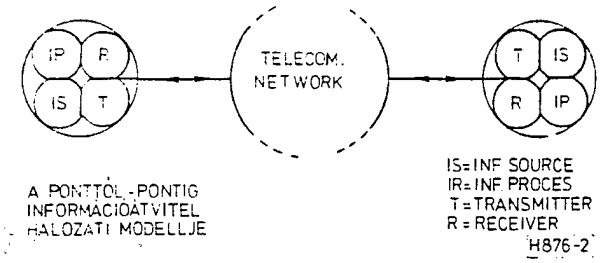

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Figure 2. Network Model of Point to Point Information Transmission

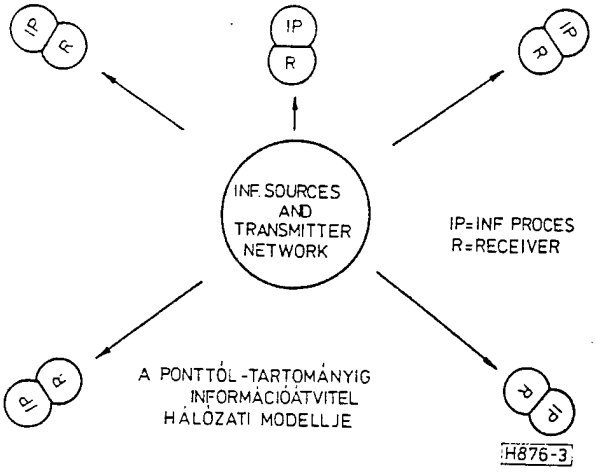

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Figure 3. Network Model of Point to Region Information Transmission

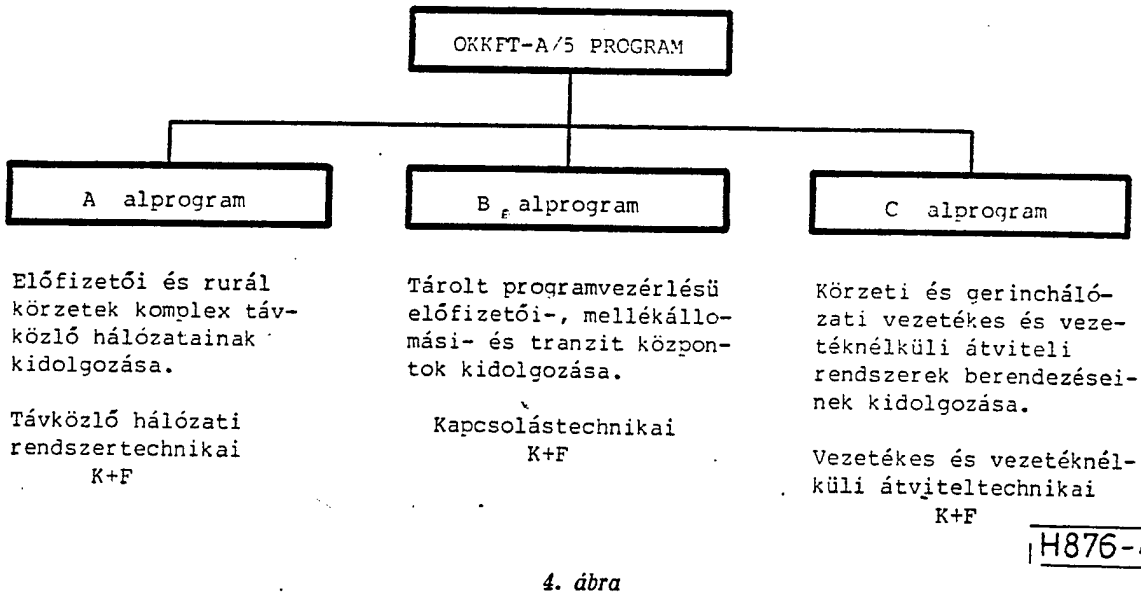

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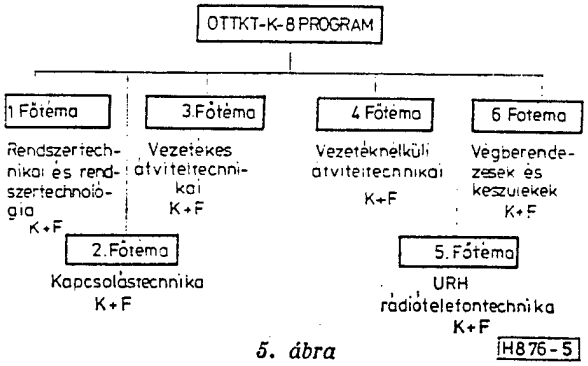
Figure 4. OKKFT A/5 Program

Sub-Program A, Telecommunications network system technology R & D; Development of complex telecommunications nets for subscriber and rural areas.

Sub-Program B, Switching technique R and D; Development of Stored Program controlled subscriber, substation and transit centers.

Sub-Program C, Landline and wireless transmission technology R and D; Development of equipment for zone and spine network landline and wireless transmission systems.



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/Figure 5 headline on following page/

Figure 5. OTTKT K/8 Program

Main Theme 1. Systems technique and systems technology R&D
Main Theme 2. Switching technology R&D
Main Theme 3. Landline transmission technology R&D
Main Theme 4. Wireless transmission technology R&D
Main Theme 5. Ultra short wave radio telephone technology R&D
Main Theme 6. End equipment and apparatus R&D

Figure 6.

IPM OMFB
MP
BME KKVMF
TKI
BHG BRG FMV HTV MEV MM ORION TERTE
OKKFT A/5 and OTTKT K/8

IPM, Ministry of Industry
OMFB, National Technical Development Committee
MP, Hungarian Post Office
BME, Budapest Technical University
KKVMF, Kalman Kando Electrical Industry Technical College
TKI, Telecommunications Research Institute
BHG, Beloiannisz Telecommunications Factory
BRG, Budapest Radio Technology Factory
FMV, Precision Mechanics Enterprise
HTV, Signal Technology Enterprise
MEV, Microelectronics Enterprise
MM, /expansion unknown/
ORION, Orion
TERTE, Telephone Factory
OKKFT, National Medium Range Research and Development Plan
OTTKT, National Long Range Scientific Research Plan

8984
CSO: 2502/24

SWITCHING TECHNOLOGY DEVELOPMENTS AT BELOIANNISZ TELECOMMUNICATIONS FACTORY

Budapest HIRADASTECHNIKA in Hungarian No 8-9, 1983 pp 348-350, manuscript received 16 May 83

EISLER, Peter, Dr. Beloiannisz Telecommunications Factory

/Abstract/ Switching technology products at the BHG [Beloiannisz Telecommunications Factory/ can be divided into two groups--subexchanges, developed on their own, and a main exchange family, produced on the basis of license know-how. Series manufacture of the last electromechanical subexchange family, the RX system, began in 1981. Series manufacture of the QA 96, a quasielectronic subexchange, based largely on domestic parts, began in 1979. The prototype of the EP 128 electronic analog medium capacity subexchange was prepared in 1980. Series manufacture of a large capacity version, the EP 512, will begin this year. PCM technology received greater emphasis beginning in 1980. Series manufacture of a microprocessor controlled small capacity digital subexchange, the EA 100, is planned for 1984. The manufacture of main exchanges is based on a license purchased from the Swedish Ericsson firm in 1968. This AR equipment has been sold to the GDR, Poland, Czechoslovakia, Cuba and South Yemen. Since 1966 the BHG has produded ATSZK 100/2000 rural telephones exchanges exclusively for the Soviet market. The development of stored program controlled systems began in 1980 to extend the market life of the AR main exchanges. Future development of subexchanges will involve cheap office systems, microprocessor controlled digital subexchanges, hotel services and a further development of software. Future development of main exchanges will involve taking over license know-how for stored program controlled digital telephone exchanges. Products for the CEMA Uniform Switching Technology System should be manufactured by the end of the 1980's or beginning of the 1990's. Intelligent subsystem terminals and a computerized system for centralized maintenance will be developed. There will be fundamental changes in product structure at the end of the decade involving developments in electronics and software. Figures 3, no references.

8984
CSO: 2502/24

ROLE OF ORION IN DEVELOPING DOMESTIC AND INTERNATIONAL TELECOMMUNICATIONS INFRASTRUCTURE

Budapest HIRADASTECHNIKA in Hungarian No 8-9, 1983 pp 351-353, manuscript received 16 May 83

KOVACS, Laszlo, Orion Radio and Electric Enterprise

/Abstract/ Orion manufactures television and audio devices, microwave telecommunications equipment, computer terminals and data trnansmission devices. By the time manufacture of them ended in 1963 Orion had manufactured more than 2 million radio sets, and the trademark is known around the world. Manufacture and export of color television sets began in 1975 in cooperation with the West German SEL firm. Experimental manufacture of television sets capable of Teletext reception has begun. In 27 years Orion has manufactured more than 3 million television sets. Manufacture of microwave radio relay equipment began in 1965; the DM 400/6 and DM 400/32 equipment was the precursor of the PCM systems which have become the world standard. Delivery of PCM equipment began in 1979 with the RP-04/30 and the RP-2/30 in the 400 MHz and 2 GHz bands respectively. This was followed by the RP-2/120 and RP-2/120T in the 2 GHz band with a capacity of 8 Mbits per second. Manufacture of 13 GHz tertiary miltiplex systems is being prepared by adapting equipment developed in France. Frequency division multiplexing equipment represents another type of microwave radio relay equipment. Czechoslovakia used Orion FDM equipment for a large part of its microwave telecommunications network. FDM equipment is made in 6, 12 and 24 channel versions, quasi-mobile or easily installed, in the 400 MHz, 2 GHz and 7-8 GHz bands. Thus far the Soviet Union has provided the largest export market for the microwave radio relay equipment. Domestic users include the Post Office, energetics, railways and oil and gas industry. PCM equipment has been sold in Peru and the near east. Orion joined the Uniform Computer Technology System of the socialist countries in 1969, manufacturing large computer remote data processing elements and systems, data transmission modems, data transmission control equipment, alphanumeric CRT displays and the AP-64 CRT data station. Remote data processing equipment is exported to the GDR and Soviet Union and to the near and far east. The flexibility of the microprocessor system used in the ADP-2052 display family makes possible the manufacture of a number of versions. Independent development of a 2 x 2400 bit/s modem on the basis of the CCITT V.22bis standard will improve the international competitiveness of the previous

AM-12TD modem. Most recently development of a 4800 bit/s modem will represent a breakthrough of the embargo on data transmission modems. A contract signed at the 1983 Leipzig Spring Fair will involve delivery to the GDR of upwards of 500 AM-2400 modems per year. The videotex program will make it possible for society as a whole to access professional computer data banks. Problems include the supply of parts and the unrealistically high domestic prices for electronic parts, which reduces the competitiveness of the end products.

8984
CSO: 2502/24

DEVELOPMENTAL TRENDS OF LANDLINE TRANSMISSION TECHNOLOGY AT THE TELEPHONE FACTORY

Budapest HIRADASTECHNIKA in Hungarian No 8-9, 1983 pp 354-357, manuscript received 16 May 83

SZALAY, Tibor, Telephone Factory

/Abstract/ The Telephone Factory is one of the largest manufacturers and shippers of landline transmission equipment in the CEMA countries. Such equipment makes up 68 percent of enterprise sales. The division of this equipment is as follows: 40 percent large channel number analog, 44 percent small channel number analog, 4 percent PCM, 3 percent telegraph and 9 percent other. The division of sales is as follows: 63 percent socialist export, 6 percent non-socialist export and 31 percent domestic. (The above figures are for 1982.) The factory manufactures 3 and 12 channel overhead line equipment, two versions of 60 channel systems using dual symmetric cable, 300, 960 and 2,700 channel systems using symmetric cable, a complete variety of multiplex equipment for connection to radio relay lines, from 12 to 2,700 channels, a coaxial cable 300 channel carrier frequency system, a 30 channel primary PCM system and a frequency modulated telegraph system with speeds of 50, 100 and 200 baud, among others. A representative survey conducted in 1982 proved that there is no substantial backwardness from the world level in regard to technical parameters and technical services. But there are problems with consumption, size, weight, reliability, the quality of customer services and the price. These negative factors can be attributed to the parts base and parts technology, and a substantial improvement would involve a sudden increase in the capitalist import proportion. It has been decided to continue to develop analog transmission equipment. There are no plans to increase variety substantially; there is no justification for increasing channel numbers up to the 10,800 channel range. Development will concentrate on satisfying special customer needs, such as 120 and 480 channel systems, primarily mono-coaxial cable and 10 channel systems in subscriber networks. PCM techology must be dealt with more intensively, but domestic production of the necessary parts cannot be expected for a number of years. A license to be purchased in 1983 will cover some PCM equipment and the purchase of equipment to manufacture thick layer hybrid integrated circuits used in PCM circuits. The Telephone Factory represents Hungary in the CEMA work to develop a uniform digital transmission technology system. Soviet-Hungarian bilateral cooperation is also important. Development of a system meeting the CCITT R 101 standard has begun. Despite investment and acquisition restrictions the Telephone Factory hopes to eventually manufacture optical cable systems with speeds of 34 Mbit/sec and 140 Mbit/sec. The

Telephone Factory will have to rely on a research and development base outside the factory to realize these goals, making use of a domestic and international division of labor, especially in regard to optical cable and PCM systems. Figures 3, no references.

8984
CSO: 2502/24

DEVELOPMENT OF COMPUTER CENTERS, EQUIPMENT DESCRIBED

Problems of Computer Centers

Warsaw PRZEGLAD TECHNICZNY in Polish No 31, 31 Jul 83 pp 14-15

[Interview with Tadeusz Mazurkiewicz, Director of the Main Computer Service Center, Gdansk, by Donat Zatonski: "Information Science, Life Size"; date and place not specified]

[Text] The network of the Main Computer Service Centers [ZETO] was to become a uniform system of computerized information services. Even today, the experienced personnel and equipment embraced by this network have huge potential. The problems of information science and computers as viewed from the standpoint of one such service center are discussed by the Director of the Gdansk ZETO, Tadeusz Mazurkiewicz in an interview with Donat Zatonski.

[Question] In the past month, there has been some movement in the community of computer scientists. Now and again one hears the rumor that some computer centers will have to be closed, namely, those that prove unable to support themselves. At your center, the self-sufficiency principle also operates, but, apparently, the Gdansk ZETO copes well. Is this true?

[Answer] We are not threatened with bankruptcy. There is no need to let people go. On the contrary, we see in the next year hiring more people, because some of our contracts are now entering a phase which will call for more personnel. However, within the area of my direct observation I know of computer centers which survive for no apparent reason.

[Question] How can one compare the customers, for instance, 10 years ago, and current clients of mid-1983?

[Answer] There are fewer of them today. There was a time when the user was looking for computer centers whatever his incentives, whether by recommendation or a fashion for this kind of "technological process" or illustory hopes of easy results. Today we are looking for clients, and I am surprised to discover that the most popular type of system with customers are prosaic ones: financial bookkeeping, payroll, inventory management, etc. I explain

this by the fact that many of our customers experience shortages of bookkeeping, accounting and similar personnel.

[Question] For almost a quarter of a century, information science and computers have been looking for a place in our society, and now it turns out that the most popular systems are those most elementary, as you have said, "prosaic."

[Answer] Yes, these are the most elementary documentation systems. But this is no treason to complain--that they are so trivial. After all, documentation systems are responsible for collection and ordering of data. These data are the base of higher administration systems--decision-making and government. Such have been the dreams of our decision-makers at various levels. Today the attitude of clients towards computers is very rational, although--I must admit--some of the past "traditional" attitudes have not vanished: departmental feuds and barriers, departmental isolationism--these are still observed and continue to make implementation of the economic reform difficult.

[Question] How does this concern information science and, specifically, your ZETO?

[Answer] In the areas where there is a large number of computers, and the coastal regions belong to this group, there is a real competition of prices and quality of service in information science ...

[Question] ... But this is very good!

[Answer] Yes, this is very good! Except that competition is sometimes handicapped by the epigons of the old system, where all kinds of connections and systems weigh more than economic considerations. For instance, although my services are cheaper and better, a certain customer would use the computer center within his departmental sphere, because either he believes this is the proper thing to do or because his colleague works there to whom he wants to give a chance to make a profit, etc.

[Question] Life has taught these people to use a certain savvy, and it's not surprising that they attach more importance to their "connections" than to economic calculations. In the long term, one never knows what pays better. Generally, however, I am getting the impression that you are complaining. Has your center been mistreated?

[Answer] We have rushed to believe in the reform and have been slightly penalized for that. All in all, we do not blame these experiences on anyone. We are still competitive in terms of price, and this fact is beginning to weigh more with clients, although a little too late ...

In 1981 and 1982, we did not change the prices at our ZETO. We figured that, when everybody around us raises their prices, we will have a competitive edge. As it turned out, our competitors brought nice results, and only a small number of clients actually gave much thought to prices. Today we see

that the situation has changed slightly in the economy. Everywhere one begins to see how people are guided by economic calculations in their activities.

[Question] From what you are telling me, it seems that there have been no dramatic changes in the mentality and attitude of clients to computer services, except there are fewer of them and they are more cautious about spending.

[Answer] Another new phenomenon is worth mentioning. Over several decades there has been major progress in computer electronics around the world. Besides the large computers, minicomputers have become popular, and also microprocessors--inexpensive, efficient, small units, using very little energy and designed for specific operations and functions--have gained wide popularity. This is a new trend in the world. It seems to me that in Poland this still remains a matter for the 1990's. Currently, however, an increasing number of our clients are beginning to ask about minicomputers.

[Question] A new fad?

[Answer] There may be a rational core in this curiosity, but in this development we feel the old conviction that having one's "own" computer allows one to utilize it effectively. When a client pays us for a service, he sees black and white what our profit is, which is not much--15 to 20 percent. So he figures that if he had his own computer ... etc., etc. He forgets about the cost. Practice so far shows that the real computer service costs at in-house enterprises are not easy to estimate, because they are dissolved in general enterprise costs. As a leftover from the past, there still is this opinion that having one's own computer is better, and since there is a shortage of money, people are thinking of buying a minicomputer.

[Question] This continuing longing for their own computer base on the part of enterprises menaces your interests--so you are critical?

[Answer] If I shared the old philosophy that would be true, I should be concerned. But today there is nothing to prevent our ZETO from embarking on delivery of equipment, for instance, under contracts with GDR's Robotron. We can also produce software and sell it with minicomputers. After all, we not only have computers that we use for calculations, but a well-educated, highly skilled professional cadre of programmers and system designers.

[Question] You have mentioned that clients are beginning to order services that they believe to be necessary, but who makes these decisions?

[Answer] The reductions of spending on computer services that could be cut started from the time of creation of workers' councils. In many cases, they required breaking the contracts with computer centers, and in some cases that meant giving up systems which were in fact necessary for the factories.

[Question] Do you think that such instances were an upshot of the belief that information science and computerization are in general wasteful, or simply that the aim was to cut on costs at any price?

[Answer] In most cases, costs were the basic argument. However, I am familiar with the decision of a workers' council to rescind a contract for operation of a system that made it more difficult for the employees to abuse their positions. This was a distributor company which carried on its activities with a pecular flexibility--"for the mutual benefit."

I have mentioned that our general partner is the client looking for documentation systems, but there also are others--those truly interested in complex management systems--which have not discontinued their projects. For instance, some projects initiated in 1980 are still continuing despite the disruptions in the economy.

[Question] Where does this consistency come from?

[Answer] I believe that this is partly to the credit of a central agency in this economic center that manages computer services. It is important to understand their real needs, because in this case it is not pressure "from above" but conscious initiative by the enterprises.

[Question] There are a few positive examples, so it would probably do no harm if you mentioned the name.

[Answer] I was thinking of Gdynia Radmor, an enterprise with a complex system of production which has been consistently working towards modern reorganization. We at the ZETO have been serving them for quite a long time. I am deeply impressed by the management of this enterprise--despite the changes in the composition of the management, the problems remain, and each new managerial board succeeds in implementing whatever is needed. In this way, with the final touches that remain to be done, we are bringing to completion a complex management system.

Another positive example is Cefarm enterprises, which is a drug distribution company. We are helping them to distribute drugs according to orders, available stock, etc. The system serving them required modernization, and it is going on in cooperation with the leading Cefarm division in Gdansk. The Cefarm association that sponsors the project has not abandoned it, despite a shortage of funds.

[Question] We are trying to rebuild the economy in an extremely difficult situation. Is this to be observed in any of the requirements of your clients, or are there signs that they have learned to use computers as a tool even in such a complicated situation?

[Answer] New assignments are being put to the systems. I am thinking of those who are going on with earlier projects. These are mainly well-managed enterprises with staffs already possessing certain informational culture. Along with modified systems of management, they are now placing orders to

us to modify the existing computerization facilities. I will admit that this gives us some trouble, but there is no way out. This situation compels us to create basically new elastic and flexible systems responsive to change.

However, new contracts for system design are few. They come from a small number of enterprises which thus far have been using primitive means of data processing or no such means at all, and now in view of personnel shortages are looking for help.

[Question] Do you not, however, feel concerned that ultimately you will be left without orders?

[Answer] I have no such apprehensions. Our assignments for the coming year are increased. Our revenues based on data processing, which account for the bulk of our income, is 70 to 80 percent, and the rest comes from system design and creation of new data carriers.

We are serving the best clients, which guarantees a stability of cooperation. These are large-scale data users such as NBP [Polish People's Bank], ZUS [Social Security Administration], PKO SA [Association of Savings Banks], PZU [General Insurance Company], Agroma, CPN, Cefarm and others. Cooperation is good, although these are demanding clients.

[Question] Not all these large-scale clients that you have mentioned are satisifed with ZETO services. For instance, ZUS has decided to rely on its own forces, and as I have heard from many computer engineers, this is a disconcerting development.

[Answer] The case of ZUS is a typical instance of mentality and actions in terms of categories of the 1970's. Since long ago, we have implemented as a ZETO network the contract on cooperation with ZUS. Things have not been running smoothly for various reasons, but this is not a sufficient argument to go to the extreme decision--this is my opinion.

ZUS has major organizational problems to wrestle with and wants to do this with the aid of computers, but according to the well-known principle: Why should I resolve my problems by other facilities when I can have my own. In fact, ZUS has hard currency reserves and could easily decide to buy minicomputers. As an association of ZETO enterprises, we offered our contributions, which have been discussed with the industry, which confirmed that it can provide the necessary domestic equipment at a minor spending of dollars. We offered several alternatives of the entire system organization to ZUS, starting from their having only terminals to complete equipment with domestic minicomputers.

[Question] I am not surprised that ZUS has no trust in "guarantees" as regards "initial consultations" with our computer industry. The matter of payment of pensions and benefits is something more serious than keeping telephone or utility bills. This is a problem of highest social rank, and hence their decision to prefer creating their own guarantees.

[Answer] I realize that this is a matter of major social significance. If, however, ZUS wants to create its own computer facilities at its 55 branches then indeed organizing such a network on the basis of domestic equipment might be difficult and risky. However, deciding to purchase equipment in the West using the models of similar networks in Western economic conditions is also taking a risk. ZUS has no proper technical organization to service this equipment. In Poland, we do not have producer services, which should be considered when making such purchases. Even if this service would be instituted for these 50 to 60 minicomputers, we will have to pay for it with dollars. Hundreds of employees will have to be hired, and centralized stores of operational material kept. Simply, they will have to create a new network of computer facilities which at more than 50 locations would employ each several skilled technicians. I may not know the details of this undertaking, but it seems to me that--in our conditions--this is destructive.

On the other hand, as a ZETO we are an organization that could serve ZUS throughout the nation, because we are already doing this in the area of payment of pensions and benefits and their reevaluation. We are also serving banks and savings institutions. Between 6:00 and 7:00 a.m. daily we provide printouts of all accounts, and do this over the territory of nearly the entire nation. No one can therefore claim that the ZETO organization is "inadequate" for this task.

[Question] I admit that I would not presume to arbitrate in the matter of ZUS. I have mentioned, however, that since you are concerned about the interests of your firm you would not object that this is both an emotional and a financial issue.

[Answer] I have no intention of denying that ZUS is a very good client, which has been systematically using our machinery. However, if I have been slightly carried away by the issue, this is so because I have been thinking of the recent past, when so many so-called complex ministerial, industrial or other sectoral systems broke down. Nothing happened besides buying equipment, spending millions of dollars on purchases and millions of zlotys on design and programming.

[Question] I want to mention again the doubts, which are not only mine, that our computer industry is incapable of meeting the nation's equipment needs. I am not saying that this is not possible!

[Answer] This is true. When I come to the Poznan Fair and look at the exhibits of Polish producers, I begin to have hopes ... But this solution is quickly dispelled when it comes to purchasing transactions. There is still a great difference between the "exhibition period" and "store inventory" with suppliers of this equipment. Personally, however, I have no reason to complain, because our center is in slightly better situation than others. We have accumulated early on a large amount of equipment. We have spent a lot of money educating personnel in how to service our technology. Thanks to this, the operability of our computers is one of the best in Poland, and the down time accounts for 5 to 6 percent of three-shift operation. On the other hand, it is a fact that our equipment is

already obsolete, and our Odra 1305's are seven to eight years old.

[Question] How long do you estimate you can provide services with this equipment?

[Answer] As long as this will be necessary, but for this work to be sensible we must have new equipment in 4 or 5 years.

[Question] Do you realize that the time-honored Odra will have to be replaced by Ryad computers?

[Answer] This is no surprise to us. After the Ryad family of computers appeared, we proposed cooperation to Wroclaw Elwro. This was a project for transition from Odra software systems to Ryad. Or, more exactly, developing a simulator so as to be able to use programs written for Odra to operate Ryad computers. After all, we cannot allow major efforts being spent in the entire nation on writing programs for Odra to go to waste.

[Question] I attended a conference where users of computer equipment called upon Elwro to produce such simulators, aware that this is an important element of transition to the new generation of machines. As far as I recall, this never came to more than promises ...

[Answer] In 1979, at the Fourth National Conference of Computer Scientists in Wroclaw, we exhibited the first simulator model. Even then we proposed cooperation to Elwro in this area, and a project was even contracted by the then Mera association, but nothing happened.

[Question] Maybe indeed you were too weak a partner?

[Answer] Not in this area. We have problems resolved today on which Elwro specialists are just beginning to work. According to their own estimates, they do not expect results soon. At the conference in Wroclaw, they promised to develop a simulator by 1986, while we will offer it for sale in the fall of 1983.

[Question] Are you not being overconfident; a stance like that should be substantiated.

[Answer] World manufacturers of computer equipment also have design bureaus developing standard programs and user programs. Elwro from the very start dissociated itself from this work, so that functions in programming were partly taken over by the ZETO network. Elwro had its own research and development center, though, which was largely concerned with programming, but this was a unit that had ambitions of being an academic institution and soon grew over into a bureaucracy tending to attack problems on a "broad front" instead of concentrating on issues important for users in a logical sequence. This is an opinion based on observations over many years and numerous attempts at establishing contacts. As soon as a competitor appeared in any related specialty, and examples are numerous at ZETO, that center, instead of collaborating with them, either ignored

them or even in extreme cases obstructed their activities. I see no rational explanation for such behavior, except the attitude caused by a monopoly position of the producer and sheer ambition.

Meritum-1 Personal Computer

Warsaw PRZEGLAD TECHNICZNY in Polish No 48, 27 Nov 83 p 31

[Article by Roman Dawidson: "Personal Computer"]

[Text] It happened! We have the first Polish personal computer. The unit has been exhibited at the 41st National Fair "Fall 83."

Our editors have been invited to visit the booth of Mera-Elzab and Foreign-Polonia Enterprise ITM in Poznan, where their joint product was to be shown. The latest fad in electronic equipment, Meritum-1, or, as it is called throughout the world, the personal computer.

To tell the truth, I was astonished by this news. Observing the developments in Polish electronics, I did not expect such equipment to appear on our market in the near future. Who would need a personal computer? A scientist never knowing where to get a component he needs for tomorrow's experiment or where to borrow a journal he wanted to read? An engineer, who after a day of fighting for maintaining production levels comes home and, if happens to turn anything on, that would be his television? Or a housewife ... ?

I must admit that I have underestimated the drive towards modernization that permeates our society. Crowds were churning around the booth where Meritum-1 was being shown. The question, "Where can this be bought?" was heard from all sides.

A few words about the unit. Meritum-1 is a basic model. The user can build up the system by purchasing additional components and developing the software. The configuration is based on microprocessor Z-80. The memory contains 14 K bytes of EPROM memory and 16 or 17 K bytes of RAM memory. The keyboard has a typical structure (QWERTY type).

The system consists of the computer, the voltage amplifier (housed in a separate unit), ordinary black-and-white television display unit and a cassette recorded with usual magnetic tape cassettes as information carriers for program and data files. The computer is programmed in an expanded version of BASIC language. It has also vast programming capacities, allowing it to write, activate and update programs. The version of BASIC language for the Meritum-1 contains a set of operation instructions on interchangeable circuits, in particular enabling communication with the program in the internal language of microprocessor Z-80. The use of television display makes it possible to present information in a graphic form.

The idea of developing a personal computer originated at the Foreign-Polonia Enterprise ITM. Yet, it is, as known to all designers, from concept to pro-

duction a long way. ITM had two alternative solutions from which to choose: either start producing the system itself or farm it out to a specialized factory. The latter path was chosen. The manufacturing was undertaken by Enterprises of Computer Equipment Mera-Elzab in Zabrze. The ITM enterprise handed over the design it developed, retaining the sales of software and further work in development of the system in its own hands. What was gained? It obtained experience, partners (designers), as well as operative production line, skilled personnel and, most important, access to components produced by domestic industry. Our personal computer is built of components manufactured either in Poland or in CEMA nations. In particular, the working dynamic memory and long-term memory are Soviet manufactured, and the microprocessor comes from the GDR.

Before the end of 1983, Mera-Elzab will put out 50 minicomputers. Next year they will put out 1000 ... and in 1985, 5000 units.

Evaluating the projected development of output, we should return to the question as to who is going to buy the appliance. Who and for how much? The price of the computer without the cassette recorder and the television display has been set at 100,000 zlotys. Is it expensive or cheap? If I wanted to buy myself a partner with whom to play chess or a toy as a pastime to fill long fall and winter evenings, this is expensive, although I assume that such amateurs will also be found. This was obviously the opinion of traders from Opole, who ordered 20 personal minicomputers. They are going to put it on sale in the store that will open next year. Were they right or wrong--we will see.

Most interest for the personal computer is found among craftsmen. An increasing number of people of a higher educational and professional level are now employed in crafts. I asked one of them what he would need a minicomputer for. I received the following answer: "I have several employees. I must keep documentation, register time of work, leaves and vacations. I have to keep accounting books and have a warehouse with a large number of spare parts and components necessary for production. I make use of a large number of catalogues, etc. Currently, all this work is done in my workshop by two employees. If their average salary is about 10,000, you can easily estimate how fast this cost will be amortized."

Designers foresee also other applications, for instance, in design bureaus for engineering calculations. Memorizing, processing and presenting collections of data such as card files, patient registers and reference information, the computer will serve for control of medical equipment such as artificial kidneys. And, of course, its software includes a set of games such as chess, Mastermind, educational and skill-developing games.

I believe that the personal computer Meritum-1 gives a chance to break the Polish society's "illiteracy" and help acquire skills in using computer facilities. The average high school and even college graduate, and sometimes, embarrassing as it sounds, engineers, have no idea of how to use a minicomputer. I am not speaking of the knowledge of the principles of its operation, but just about the practical skills of using the computer

as a tool. In many countries, these skills are acquired in high school. In Poland, we do not provide such education because of the cost, for instance, of a minicomputer. We now have a new opportunity: 100,000 zlotys is not a major outlay for a high school, even in a small town, and there is hardly a school that would not have a television set or cassette recorder. So the complete system will be ready. This way, a school's "computer center" could be created to teach the young people, who could carry out there, for practice, such tasks as compiling a computerized catalogue of school library, a register of students, etc. There is no limit to ideas and possibilities.

The Ministry of Education should start even today negotiations with the manufacturers and programmers as to the number of units it might need, the development of BASIC software and the methods of training teachers of mathematics.

Interest among young people is tremendous. Teenagers hung around the Mera booth and learned how to use the Meritum-1 after just a few tries.

As the manufacturers wrote in their promotional hand-out: "Buy Meritum-1. At work it will help you with a laborious algebraic equation. It will edit and print 47 copies of conference notices. At home it will help your son practice his skills in BASIC language or play a computer game, and in the evening it will be your partner for a game of chess."

Designers of the personal computer Meritum-1 are Jacek Lipowski and Pawel Podsiadlo, Foreign-Polonia Enterprise ITM, and Zygmunt Korga, Chief Designer, Mera-Elzab Enterprise.

Decline in Computer Equipment

Warsaw RZECZPOSPOLITA in Polish 17-18 Dec 83 p 4

[Article by (al): "Prospects in Information Science"]

[Text] Interesting data are given in a report on a survey conducted at Poland's information science centers by the Center of Research and Development of the National Statistical Information System. In 1982, we produced 17 computers and 140 minicomputers and purchased abroad 19 computers, selling 2 units of the Odra 1305.

The survey embraced 1432 information science centers. In 1981, there were 166 more of them. The reasons for closing of some were mainly reduced computer services at many institutions, dismissal of employees and sale of equipment. The less efficient and operative equipment was registered mainly at higher schools, where an increase of the number of centers has been observed.

The employment at centers is declining. At 158 self-sustaining centers, the number of employees was 20,500, with just 25,471 individuals staffing the remaining 1284 centers (an average of less than 20 employees per center). Given the total number of 2553 operative computers, the status of

computer hardware in four main economic-type ministries has declined (from 51.4 percent in 1981 to 48.8 percent in 1982). Experts emphasize that the main cause for this situation is wear of computers (average service life of 6 to 8 years). Average salary in the industry was 8,995 zlotys.

Lightweight Computer Disks, Hardware

Warsaw KURIER POLSKI in Polish 6 Sep 83 p 2

[Article by (raw): "Computer Disks Lose Weight"]

[Text] In the electronics and computer industry, the savings program has direct connections to technological progress. At Krakow Measurement Instrumentation Factory, two new solutions have been developed that will allow (starting next year) savings of a large quantity of valuable material.

Currently, a computer memory unit on floppy disks weighs 10 kg. The new disks will weigh just one-sixth of that, that is, 1.5 kg. The higher generation of electronic components, microamplifiers, replacement of machining by plastic forming, new readout heads and other innovations will result in a fourfold productivity increase.

The situation is similar with the microcomputer. Until now, its weight has been 130 kg. After the "weight loss diet" its weight will go down to 30 kg. Thanks to these solutions, we are coming closer to the modern accomplishments of world computer technology.

Contractors from socialist countries, informed of the new specifications of the prototypes, said they would like to use them. Both new solutions of the factory, therefore, are likely to become export commodities. The output increase planned for 1983 and 1984 will be to 30 percent fulfilled thanks to saved materials.

Minicomputer System GS-80

Szczecin KURIER SECZECINSKI in Polish 26 Sep 83 p 3

[Article by (wab): "A Conference at Szczecin Polytechnic: Computers in Industry"]

[Text] Last Friday, the Second National Conference on "Computer Applications in Industry" organized on the initiative of the Scientific and Technical Committee for Information Science at the Szczecin Province Science, Technology and Education Department, held its final sessions in the building of Technology and Chemical Engineering, Department of Szczecin Polytechnic.

The conference had heard over 90 reports and communications by engineers, economists, mathematicians, teachers from higher schools and scientists from academic research institutions. It also awarded prizes for a contest

for the best industrial implementation of computer systems. The first prize was awarded to the staff of the Gdansk Polytechnic Information Science Institute for development of a minicomputer system GD-80 for automatic testing of internal combustion engines. The project has already been put into practical use in the automotive industry.

The second prize was given to scientists from the Institute of Nuclear Chemistry and Technology in Warsaw for the project of a mobile laboratory for investigation of dynamic phenomena in industrial processes and technological installations. The third prize was received by Christoph Grajek, from OBRUM [expansion unknown], Gliwice, who developed an automatic graphic unit for design analysis by the method of modular elements.

In its final document, participants of the conference emphasized the need to increase the interest of producers in computer system productivity, improved computerized information services and dissemination of knowledge in this area. The next conference has been scheduled to be held in Szczecin in two years' time.

Text-Editing Computer Screen

Krakow ECHO KRAKOWA in Polish 23-25 Sep 83 pp 1, 2

[Communication by Polish Press Agency: "A New Development at Warsaw Polytechnic: Text on Screen"]

[Text] A series of monitors has been developed at Warsaw Polytechnic which, connected to Mera-4 computers, allows to edit text on a screen. The display design has been developed at the Automatics Institute of Warsaw Polytechnic. After tests, the production of units has been started for the Institute of Meteorology and Water Management at Krakow.

Screen displays permitting editing of texts are already being produced in Poland by Elzab Enterprises in Zabrze, but the Warsaw Polytechnic design has higher technological capacities.

The units allow editing of texts on the screen from a digital computer memory. Using equipment popular in many countries, the system will be found helpful by editors, publishers, etc. The electronic equipment can edit, memorize text and do line breaks.

Publishers in Poland have shown interest in Warsaw Polytechnic's design with a view toward computerizing book publishing. For the moment, however, the screen monitor is used by the Polytechnic itself--a configuration linking the monitor to the computer is operational now at the Laboratory of Automatic Systems of Warsaw Polytechnic. The next units to be produced will be placed at the disposal of specialists working in the framework of government program PR-7 on problems of water management.

Computer Service Center Capability

Warsaw ZARZADANIE in Polish No 11, Nov 83 p 11

[Advertisement]

[Text] Activities in provinces: Katowice, Bielsko-Biala and Czestochow; services performed by units located in province capitals and Katowice ZETO branches in Bedzin and Gornicza Dabrowa.

Information services in the following areas: expert examination, analysis, consultation on introduction of electronic computer technology, design and programming of computer data processing systems, system introduction and operation, development of machine information media, training of staff for system introduction.

We have: 10 computers of uniform system; systems from R-20, R-22, R-32 to the largest model, R-60 (operating under DOS operation systems with POWER II and OS).

At Katowice Center, computers operate in an on-line mode.

ZETO Katowice accepts orders for products to be installed on customer's premises.

We recommend the following systems: Sygmat--inventory management; Efka--bookkeeping and financial documentation; Place--payrolls; Podest--durable goods documentation; Cefarm--drug circulation and distribution; Rejestr--regional vehicles and automobile documentation; Sarcz--percentage rate calculations; Sarifo--calculation of energy and gas consumption; Sart--automatic calculation of telecommunication services; and Emiren--pensions and benefit services.

Main Computer Service Center (ZETO) Katowice-Welnowiec, Owocowa-1.

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LONG-RANGE ELECTRONICS PROGRAM OUTLINED

Warsaw PRZEGLAD TECHNICZNY in Polish No 46, 13 Nov 83 pp 10-13

[Article by Stanislaw Stepien: "Program of Application of Electronics in the National Economy"; fourth article in a discussion series entitled "Where Is Polish Electronics Headed?"]

> [Text] In the first six months of 1983, a group of 11 authors from important and prestigious institutions prepared--with the participation of many consultants and advisors--the "Program for Application of Electronics in the National Economy in the Time Frame up to 1990." In perusing this document, I tried to find at least some traces of our response to the technical and economic menaces to which we are exposed in the world market. I haven't found any.

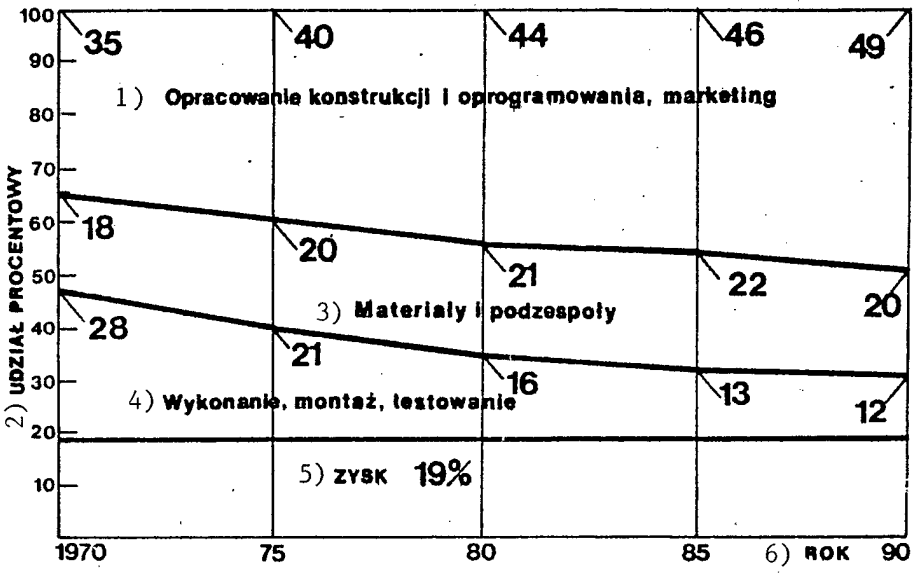
The Program contains no proposals for increasing the efficiency of the industry (productivity, dollar ratio, product quality), reducing the distance separating us from nations that are ahead or avoiding the danger of those behind catching up with us. There is no picture of our electronics industry against the world background, either currently or after implementation of this Program. All these are, however, necessary data for evaluating whether we are advancing or falling further behind.

In essence, this document confirms the opinion common among computer scientists that we lack technological perspective in the industry and virtually ignore this mandatory formula: Electronics must use ever less of ever better materials, processed ever more deeply, with ever more perfect equipment. It is no accident that investment in this area is at the bottom of the list in electronics (CNPME, UNIMA), and it is only thanks to the tenacity of the directors of these institutions that anything is done at all. Symptomatically (this is the routine style so common for a decade), in this extensive document, the authors provide no data on efficiency of application of electronics in individual industries, even though the authors are quite competent to know such data and use them to illustrate the efficiency of electronics applications.

Some of the passages in the Program deserve a closer look.

The Balance of Materials and
Subassemblies for Final Products

Worldwide, electronics is not a material-intensive industry. While the complexity of electronic equipment is unchanged, the amount of material spent to manufacture it is decreasing rapidly. Sometimes even an increased complexity of equipment (such as computers) means little rise in material expenditures (see figure), and after 1985 will even begin to decline thanks to widespread use of miniaturized electronic chips and integrated circuits in designs of carrier structures and surface assemblies (two-sided use of printed plates). For American professional equipment, the cost of materials in 1980 amounted to around 27 percent and for general-purpose equipment about 40 percent.



Key:
1. Design development, software, marketing
2. Share (percent)
3. Materials and subassemblies
4. Manufacturing, assembly, testing
5. Profits, 19 percent
6. Year

Materials-intensiveness of entire Polish electronics industry was over 53 percent, which is ahead of only two typically materials-intensive sectors: metallurgy (69 percent) and metal production (65 percent). This high materials-intensiveness of electronics also reflects:

--low efficiency of materials and subassembly production and low level of processing of materials; and

--inadequate payments for labor.

If this average is assumed to be correct for final production as well (where the bulk consists of general-purpose electronic equipment and units for electronically controlled appliances), this means that for meeting the planned amounts of end-products we will have a shortage of materials and assemblies of about 24 billion zlotys in 1984 and 40 billion zlotys in 1990 (Table 1).

Table 1. Balance of Materials and Subassemblies for Manufacture of Electronic End-Products

	Billion zlotys per year	
	1985	1990
End-products	173	285
Required materials and subassemblies	92	151
Delivered by electronics industry	53	88
By others[1]	15	23
Imported[2]	0	0
Shortfall	24	40

[1]My estimate.

[2]Minuscule import of materials for production of subassemblies and minor amounts for equipment manufacturing is envisaged from dollar markets.

Integrated Circuits

Integrated circuits of an appropriate quality level and manufactured in required amounts are key to implementation of the entire program. The authors carelessly confine themselves to giving the number of semiconductors of one group of integrated circuits which our electronics industry is likely to produce by 1990. To express the output of semiconductors in dollars, they assume that in 1990 we will be producing: 12 million units of microprocessor systems ("Program"), 60 million units of other integrated circuits, and 388 million units of discrete semiconductors. With the current liberal estimates of world prices of our semiconductors, that will amount in 1990 to about $105 million. With a population of 40 million, this means an output of about $2.6 per capita, and that only in 1990!!!

For comparison and to better understand what sort of an electronics power we shall become, it should be mentioned that in 1982 Hungary produced $3.8 per capita and the GDR about $8.

Computerization of the National Economy

"Most generally, this revolution is based on a radical growth of labor productivity of man equipped with the means of automation and information science" (Program, page 4)--this is how the authors of the Program define the concept of the microprocessor revolution.

The recipient of the Program, therefore, could expect that the measures suggested in the document confirm our intention to participate in that revolution. Practically, that means a fast growth of the supply of computerized and electronic equipment to the economy to ensure a rapid productivity growth and improvement of product quality. (For instance, for reducing the failure rate of semiconductors produced by CEMI [Semiconductor Scientific Research Center] to below 0.4 percent, a completely automated system of semiconductor testing and selection is required, according to a speaker at the 25th anniversary conference of CEMI.) Computers, which embody a high added value, are a perfect item for export. The growth of export of these products envisaged in the Program is, of course, desirable.

Of a basic importance, however, is the production of computers for improved efficiency of the national economy: however, despite a considerable increase in exports (Table 2), the share of products remaining in the country in 1985-90 will be smaller than in 1980. This is a worrisome situation, which means drastic deterioration of the production conditions and eventually increased cost and poorer quality. Nations developing the production of computers and electronic automation facilities allot a far larger proportion to their domestic needs. We can cite, for instance, the annual communications of the GDR's statistical office. That nation attains an annual growth of GNP without increased employment or increased use of materials and energy. This is achieved through growth of computerization and automation--by about 40 percent. The connection between the increase in the pace of electronic applications in industry and the resulting increased productivity of equipment is noteworthy (see box).

Table 2. Furnishing the Economy with Computers (dollars per capita)

	1980	1985	1990
POLAND			
Output	7.8	7.8	12.0
Export	3.0	4.8	9.0
Domestic demand	4.8	3.0	3.0
GDR			
Output	77.7	-	175.0
Export	55.5	-	130.0
Domestic demand	22.2	-	45.0

[Box]

In his paper presented at the seminar on "Microelectronics and Socioeconomic Development" (Jachranka, Sep 29-30, 1983) entitled "Development Pathways of Electronics," Professor B. Paszkowski cites demonstrative data on the relationship between the number of installed logical units and the productivity of technical equipment with electronic applications. For clear visualization of this tendency, I have tabulated his data. It is seen from the comparisons that in the past few years the growth rate of producitivity of equipment with electronic applications is commensurable with installation of electronic systems. Taking the growth of productivity of equipment with electronic applications for the entire period of 1960-80 and the growth in the perfection of electronic systems attained in that time (5.75), one can evaluate the relationship between the growth of perfection and productivity. For this period it is approximately equal to 4.1. In order to attain a productivity of equipment equal to 1, one has to improve the perfection of installed electronic systems fourfold.

The Relationship Between the Pace of Installation of Electronic Systems and the Growth of Productivity of Technical Equipment

	Growth rate (%)		
Years	Installation of systems	Productivity of equipment	Ratio
1950-60[1]	10	8	2
1960-70[2]	24	14	1.71
1970-80[3]	105	95	1.1

[1]electronic valves and discrete semiconductors

[2]integrated circuits of small degree of integration

[3]integrated circuits of a high degree of integration and microprocessors

Example: computerized aluminum sheet roller put into operation in the United States in 1982 requires--at the same productivity as before--half the number of service operators.

The Program does not cover a wide area of programming, but, on second thought, this is not surprising. If the nation does not receive computers and equipment for automating production, it doesn't need software.

The document also ignores the revolutionizing product of our time--the personal computer and other more "intelligent" products. We are expected to be satisfied with mere calculators.

Entertainment Electronics

The Program mentions intentions to introduce the production of modern consumer goods; the projected output and growth rates are impressive, but only at first glance. Converted to dollar equivalents[1] for this group of commodities, the projected output of entertainment electronics in 1990 per capita will be 9 percent below and consumption 19 percent less than in 1980 (Table 3).

Table 3. Consumption of Electronic Entertainment Goods (dollars per capita)

	1980	1985	1990
Output	8.2	5.30	7.5
Export	1.3	0.84	1.7
Consumption	6.9	4.46	5.8

The authors mention an intention of introducing some modern electronic entertainment products, but say that these delicatessen will be made for export. We the average citizens, then, will have to be satisfied with old-fashioned products available in smaller amounts. Our "entertainment" will be futile attempts to buy these products. Radio and television, however, will cushion the blow from this shortage. The suicidal cuts in programming committed by television and changes in radio programming have greatly reduced the need for the respective groups of equipment. We have finally lived to see the time when the "noisy" products are no longer synonyms for electronic goods, not only for teens but for adults as well.

Developing a National Telephone Network

We probably avoid assuming last place among European nations in terms of the number of telephones per 100 inhabitants, but already many say that both Yugoslavia and Rumania have left us behind.

Enthusiasm-Creating Products

An example of a product that created enthusiasm in society in the seventies was the private car. Today we know that this was a deficient luxury, and is likely to remain so in the future. Cars of a total market value of 1,500 billion zlotys spend most of the time parked in front of homes, because the nation currently lacks the cash to buy 1 million tons of its

oil in hard currency markets (some 170 million dollars), and so it will remain for some time in the future. Yet, a society must have some products to aspire to. So if we cannot travel around the world and across the nation personally, we at least must try to bring them closer to people. This can be achieved by electronics, and its latest products will fill all those aspirations which distinguish human existence from biological life of lower orders. These products can and should perform the enthusiasm-creating function. For this to happen, we must create the market for electronics. Electronic goods should not have absurdly high and prohibitive prices. The Program fails to recognize this role of electronics.

Where We Will Be in 1990?

When, by the end of 1990, we will have successfully completed the implementation of our "Program of Electronic Applications in the National Economy" in its current form, and given that the countries with which we compare our output will be equally successful in completing their electronics programs, the differences between the outputs of electronic goods in per capita expression will increase several times over (Table 4).

Table 4. Output of Electronic Products (dollars per capita)

Country	1983 Total	1983 semiconductors	1983 Computers	1990 Total	1990 semiconductors	1990 Computers	Growth rate, percent
United States	660	48[1]	240	1500 1900[2]	200 300	600 900	13.9
Japan	510	33	110	900	150	400	10.7
Poland	22.2	1.0	6.5	41.5[6]	2.6	12	10.6

[1]Including output by foreign affiliates (about 15 percent of total).

[2]From various sources.

[3]Produced by domestic manufacturers, outside parentheses; total output by all manufacturers, inside parentheses. [as published]

[4]Only installed computers. [as published]

[5]By domestic manufacturers. [as published]

[6]Assuming an improvement of dollar rate factor by at least 20 percent.

A fragmentary analysis of the Program shows that after its complete implementation:

--the output of electronic products will decline drastically--also compared to other nations; given the simultaneous decline in quality of

our products, this will mean an almost complete elimination of powerful electronics from hard currency markets, as well as a substantial depression of the competitiveness of these products in socialist countries;

--compared to other nations, the level to which our economy is equipped with the means of computerized automation will decline;

--communities will not receive any good inexpensive products typical of current and future stages of development in electronics (personal computers and video cassette recorders). Export of video cassette recorders planned in the Program means only that for each dollar earned in this transaction the industries operating better will have to add $200 in subsidies. It will be better for the nation if the electronic industry fails to meet this ambitious target;

--our nation will continue to be bypassed by developing telecommunications networks.

In sum, one is forced to say that this document could more aptly be called "A Program of Technological Stagnation of the Economy."

Conclusions

Nations developing at a rapid pace are the fastest to limit the development of materials- and energy-intensive industries.

A look at characteristic data (gross national product, per capita output of electronic products) for nations which have set different priorities in their development clearly shows the GNP level benefits for nations that develop electronics faster. I believe that these data are not accidental, and that in the near future it will be possible to formulate an effective measurable interconnection between the level of electronics industry and the growth rate of the GNP.

The avalanching demand for electronic goods helps steady and fast decline of their prices.

Manufacturing methods determine the costs and product quality. Most impressive examples of efficiency of manufacturing methods are found in electronics itself, especially in microelectronics. A silicon chip 127 mm across houses 100 semiconductor structures, equivalent to 60 million electronic elements (transistors, diodes, resistors and capacitors). Time taken to manufacture these structures and to press them into frame is less than one hour. For mounting such an electronic system of discrete elements, we would have to spend about 100,000 hours. This is longer the entire lifespan of the worker (90,000 hours).

Introduction of tape cables and insulator-held connections increases the efficiency of connection by 20 times. Specific automata place on printed plates over 0.5 million flat electronic elements within an hour, and using

computers for the design of printed circuits reduces the time of preparation of design and technological documentation by 5 to 20 times and allows major savings because of multiple utilization of data prepared for design of plates. Dimensional (track width 75 micrometers) traits of technologies used 20 years ago in the production of integrated circuits are currently possessed by printed circuits of modern computers (IBM 3081). Details of production methods are usually kept secret by companies, and so we should not be surprised that the American producers of integrated circuits were proud of their technology and experienced a real shock when, in 1980, the chairman of Northern Telecom Corporation (a US producer of military electronic equipment) published the results of studies of the quality of Japanese integrated circuits. The corporation, forced, due to short delivery terms, to purchase integrated circuits from Japan, had discovered that they were not only cheaper but also from 200 to 1200 times more failsafe than American counterpart products. This was the first time that a microelectronic shock ran through Silicon Valley. Thanks to this, we now know that the failure rate of integrated circuits produced by National Semiconductor was almost 46 times lower in mid-1982 than in mid-1978, and that the Japanese owed their quality lead to cleaner production rooms (technological equipment) and to better production discipline (mentality), as well as to faster introduction of improvements by technological personnel (quality circles).

Thanks to this shock, several American producers of integrated circuits set up their branches in Japan, and many of the new unit consulting firms are thriving from disseminating the results of analysis of Japanese electronic industry methods. In Poland, people underestimate and, furthermore, do not realize the importance of technology in ensuring high quality levels. This attitude starts from the top strata of scientists. When at the end of last year prestigious scientific institutions prepared lists of scientific and technological journals in electronics that they recommended for subscriptions from capitalist countries, of 140 titles only one was a journal concerned with technology!!!

Even one of the major technological journals for microelectronics was not included. Today only one--of the earlier subscribers--institute in Poland subscribes to a fundamental American journal, which is unique in the world in this area dealing with production of electronic elements and equipment. "Designing sophisticated intelligent systems is a task worthy of a scientist. Production is a blacksmith's work, mostly for the average technician." This is an opinion that I heard from a young brilliant scientist. No wonder that the failure rate of simple integrated circuits produced by the CEMI is 40 times higher than that of much more complex integrated circuits produced by National Semiconductor, not to mention Japanese manufacturers. If we now move from the pinnacles of science to lower levels, we notice that in the country there is no institution to develop modern technological processes for increased productivity of the electronic industry and that the only existing method of introduction of such processes at individual enterprises so far has been purchasing of licenses. At two of the best enterprises, there were no technologists among the engineering staff. It

looks as if our electronic factories do not need any highly efficient technological equipment. Producing less at higher cost rather than more and cheaper seems to be their policy. More power to them.

Structure carrier frames which provide major economies at higher levels of electronic equipment packaging are introduced into the microelectronics industry by the Krakow Center rather than by ITE Enterprises, which for almost three years failed to see the benefits of such structures for the users.

Recently, I was pleasantly surprised to discover that in Warsaw there exists an enterprise producing electronic goods which is quite different from the image of our usual electronics factory. This small enterprise in a modest location without neon lights and beautiful production halls, with modest outfitting, sells most of its products with a higher dollar conversion rate than the national average, and 2-3 times higher than in electronics. Its director even today is planning modernization of the methods of production, so as to achieve better profitability in the coming years. How untypical.

Medieval alchemists spent their lives attempting to change available metals into gold with no success, but this has been achieved--and to an even greater degree--by electronics in the second half of the twentieth century. From sand of a slightly better quality than common beach sand it produces semiconductor structures; one gram of this product costs more than one gram of gold.[2] The entire economic might of modern Japan grew from these products made of sand, a raw material that will never be in short supply. A nation that doesn't want to or cannot transmute sand into gold will never find a proper place at the table of world nations. It will never crawl from under the table where it fell because of overdeveloped heavy industry.

These sand products save large quanities of electric energy used by motors. In about three years, all alternate current motors produced in the United States will be equipped by the manufacturers with microprocessor control units reducing the consumption of electricity. Two or three years later, this will occur in Western Europe as well. Who will then want to buy our electric motors produced by CELMY or TAMELU enterprises? How much will a buyer--if there will be one--require as a discount when purchasing our products equipped with energy-wasting electric motors?

When in the late 1960's a group of enthusiasts under the leadership of one of the most dynamic scientists which at that time was affiliated with the Committee for Science and Technology, and individuals from other organizations, undertook efforts to promote the development of national electronic industry, Poland at that time lagged behind the world leaders six to eight years, and in some areas were just slightly behind Americans.

Today, 16 years before the 21st century, at a peak of development of the electronics industry, having more scientists in this area than

Taiwan and South Korea combined, having spent a lot of money on its development, Poland is 12 years behind the world leaders, and the distance is growing faster than before.

We have lost the contact with world leaders. If by the end of the 1990's --as already predicted by forecasters--half of the factories in the world will produce electronic equipment or equipment with electronic assemblies, we will be able to offer the world just raw materials extracted at an increasingly greater labor cost, a small amount of construction services, where we are confronting active competition from so-called less-developed nations, and primitive general engineering products of the past epoch, which[3] nobody finds worth producing anymore.

After our defeat in this electronics war, there appears on the banks of the Vistula in the middle of Europe a nation which does not at all fit into the European picture. The consequences of this development can easily be predicted, even today.

FOOTNOTES

1. Currently, the dollar conversion rate factor is somewhere in the area between its value at RM Finezja (220 zlotys/dollar) and OTVC Jowisz (350 zlotys/dollar).

2. The semiconductor unit of a 64 kRAM memory commonly used in the world already of a volume of about 20 cubic millimeters costs in the area of $1.50. That means $30 per gram. The current gold price is half that amount. For semiconductor structures of more sophisticated integrated circuits, the excess over gold is even higher.

3. In the 1950's, our industry manufactured the best steam locomotives in the world. About two years later, a curious correspondent discovered that we were the only nation producing such locomotives.

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END